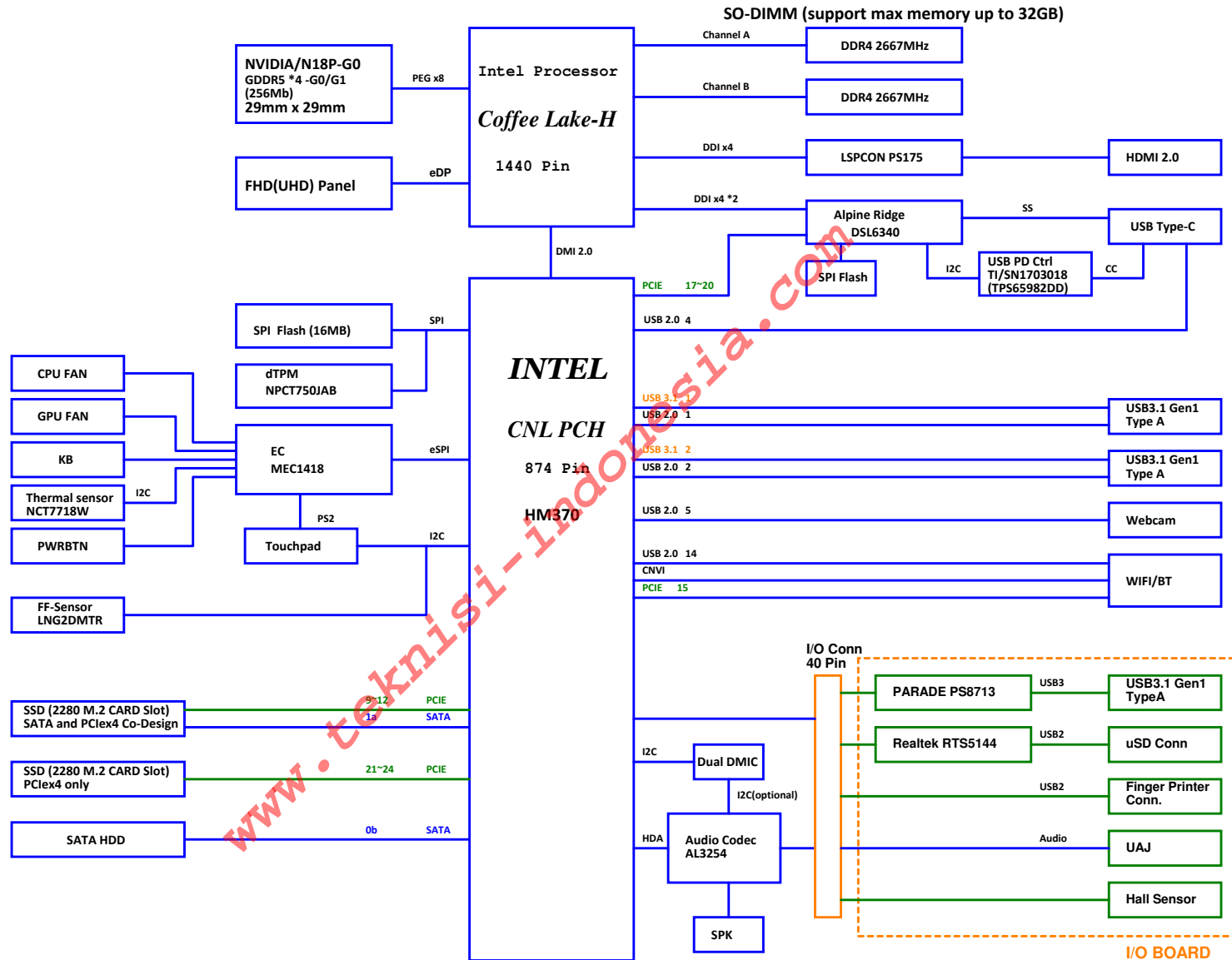
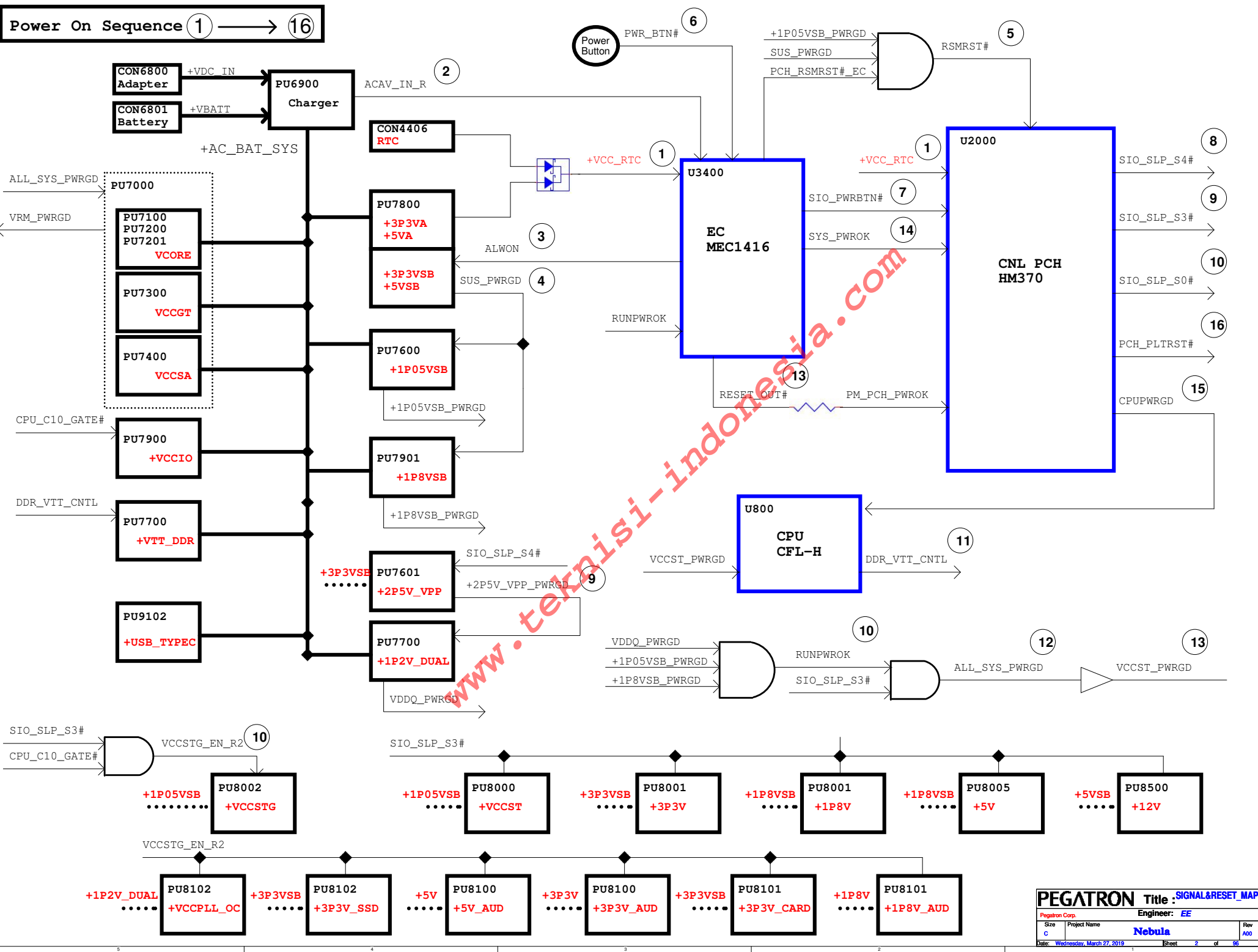


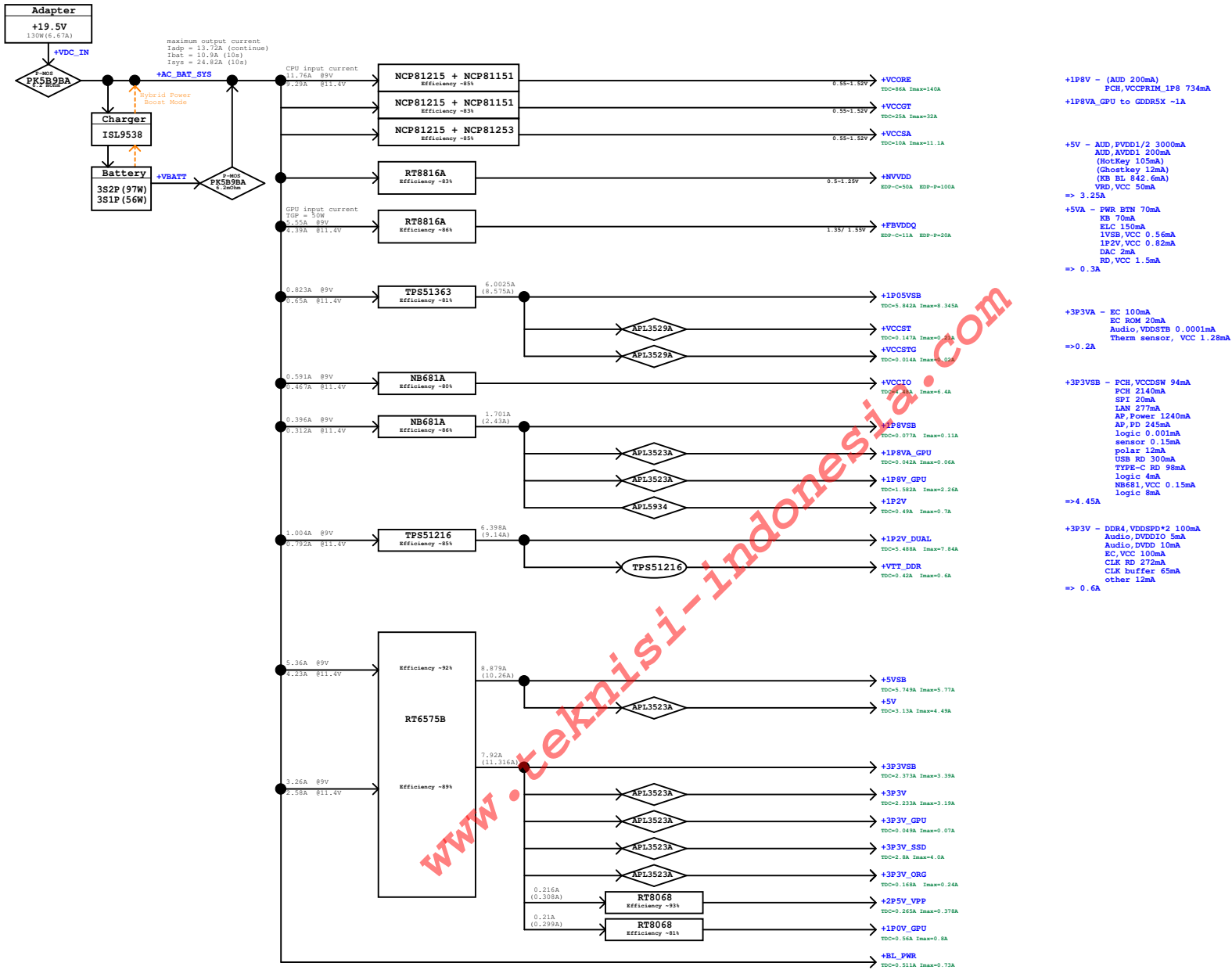
Nebula (Coffee Lake-H) Block Diagram

01.BLOCK_DIAGRAM
02.SIGNAL_&_RESET_MAP
03.POWER_FLOW_CHART
04.CHANGE_HISTORY
05.SMBus_&_I2C_Flow
06.GPU_Power_flow_&_sequence
07.POWER_SEQUENCE
08.CPU_DDI/EDP
09.CPU_DDR4_CHA
10.CPU_DDR4_CHB
11.CPU_DMI/PEG
12.CPU_MISC
13.CPU_VSS
14.CPU_POWER
15.CPU_DECOUPLING
16.XXX
17.DDR4_SO-DIMM0
18.DDR4_SO-DIMM1
19.DDR4_DECOUPLING
20.PCH_DMI_PCIE_USB_SATA(1-8)
21.PCH_SATA/PCIe(2-8)
22.PCH_ESPI/SPI/FAN/HOST(3-8)
23.PCH_AUDIO/CL/I2C/UART(4-8)
24.PCH_SML/I2C/MISC(5-8)
25.PCH_CLOCK(6-8)
26.PCH_VCC/PLL(7-8)
27.PCH_VSS(8-8)
28.Alpine-Ridge--controller
29.Alpine-Ridge--Power
30.TYPE-C_PD1
31.M.2_PCIE_X4_#1
32.M.2_PCIE_X4_#2
33.M.2_WLAN_KEY-E
34.EC_MEC1416
35.SATA_HDD/KeyBoard
36.POWER_SENSE_MAX34417
37.Enhance_LCD_BIST_&_MBIS
38.USB_CONN_&_POWER
39.SENSOR
40.AUDIO_AL3254
41.SPEAKER_CONN
42.TPM
43.SM_BUS_&_SPI_ROM
44.Other_CONN
45.ACAV_IN
46.LID_Open_PWR_ON
47.PCB_&_Label_&_Screw
48.eDP_CON
49.ClickPad
50.XXX
51.HDMI_2.0--LSPCON
52.GPU_PCIE
53.GPU_FRAME_BUFFER
54.GPU_XTAL
55.GPU_HDMI
56.GPU_GPIO_STRAP
57.GPU_Power_GND
58.GDDR5_256M_x32bit_A
59.GDDR5_256M_x32bit_B
60.GPU_XXX
61.GPU_XXX
62.GPU_XXX
63.GPU_XXX
64.GPU_XXX
65.GPU_XXX
66.GPU_XXX
67.GPU-POWER_Sequence
68.DC_IN
69.Charger
70.VR_CONTROLLER
71.Vcore_Driver-1
72.Vcore_Driver-2
73.VccGT_Driver
74.VccSA_Driver
75.Vcore_&_VccGT_CAP
76.+1P05VSB/+2P5VPP
77.+1P2V_DUAL_&_+VTTDDR
78.+3P3VSB_+5VSB
79.+VCCIO_+1P8VSB
80.Load_switch_1
81.Load_switch_2
82.+NVVDD_Controller
83.XXXX
84.XXXX
85.XXXX
86.+FBVDDQ
87.+1P0V_GPU/+1P8V_GPU
88.GPU_POWER_CAP
89.GPU_POWER_DISCHARGE



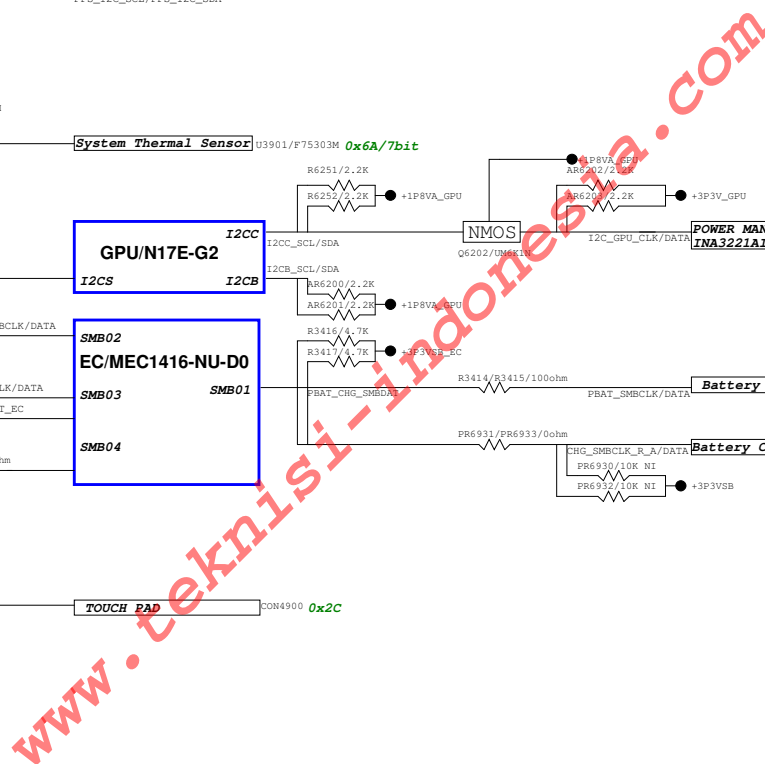
Power On Sequence ① → ⑫

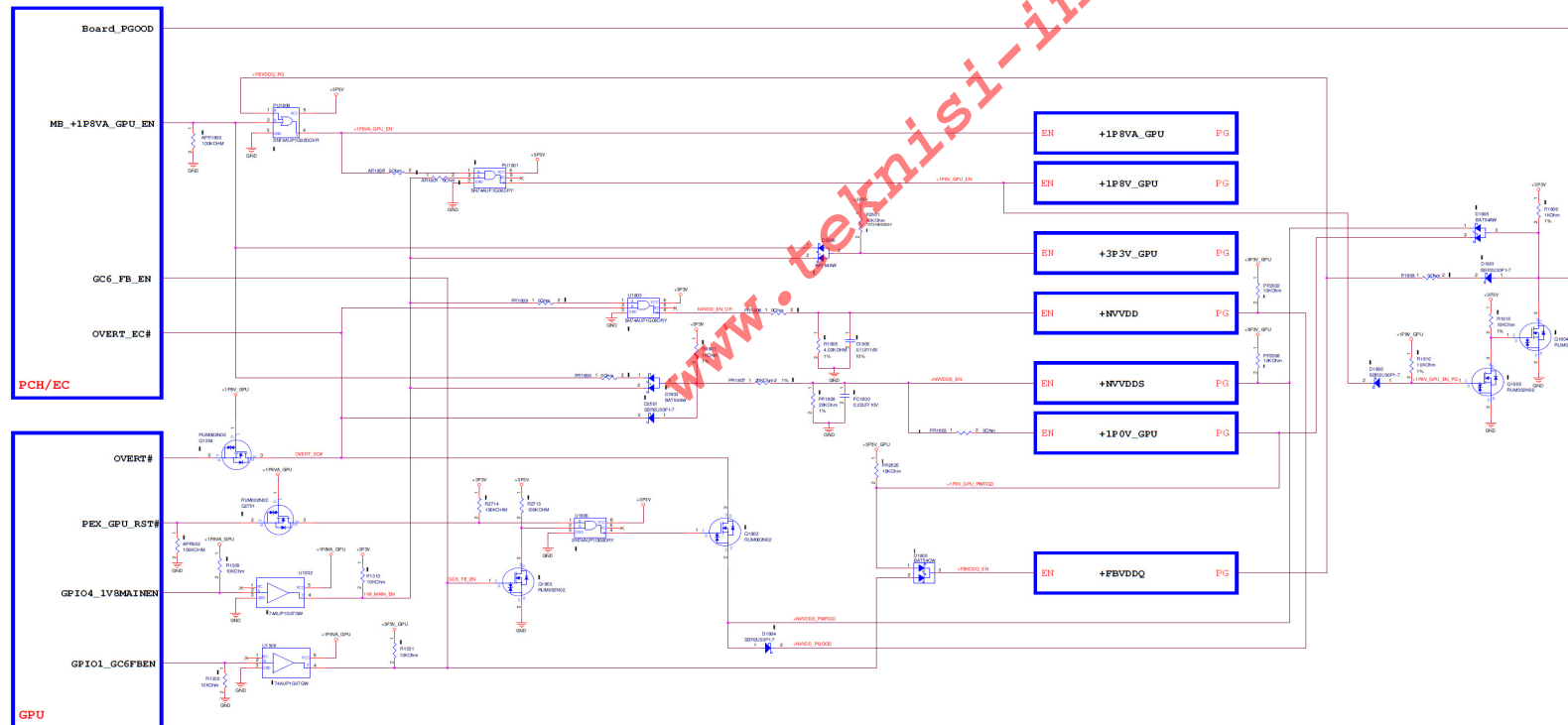
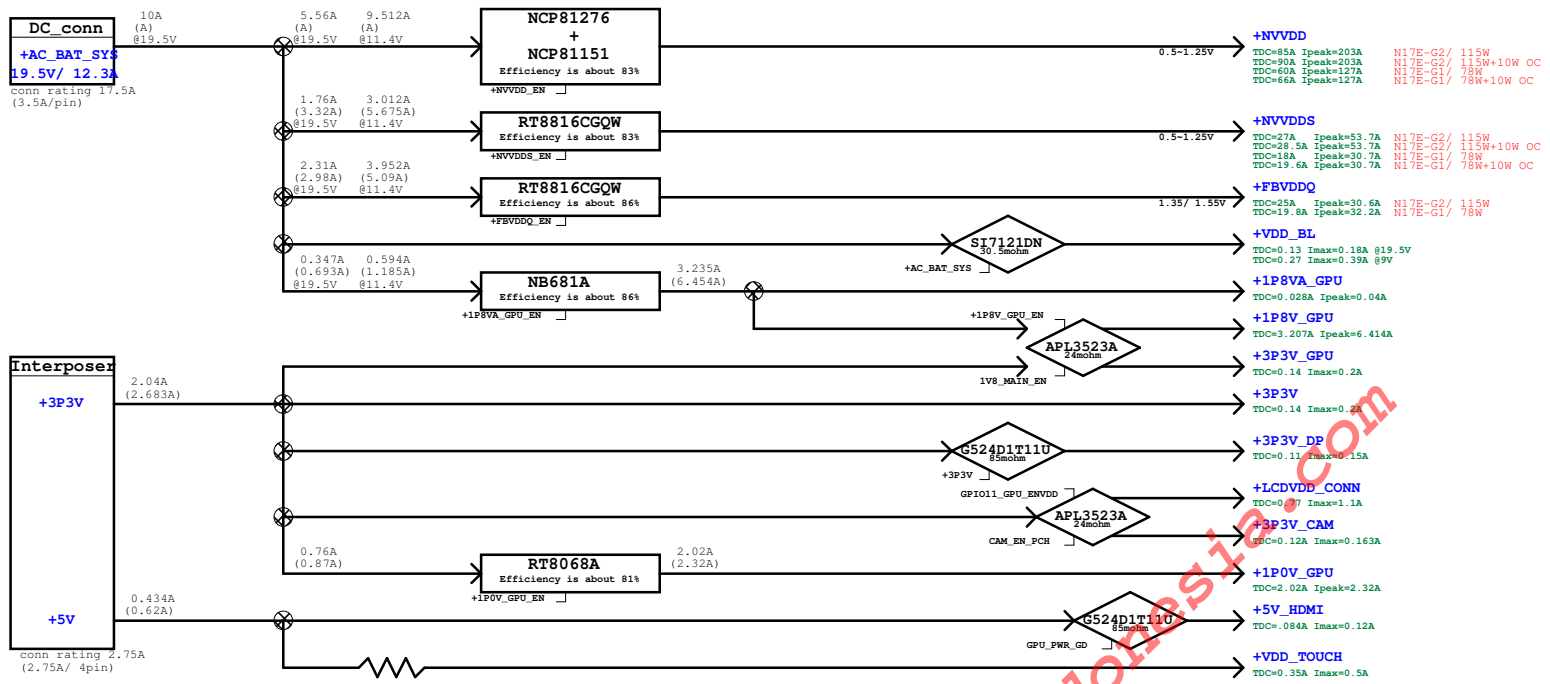




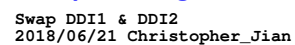
[illegible]

PCH





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U0800D

28 DDI2_TXP_0 <<< K36 DDI1_TXP[0] EDP_TXP[0] D29 >>> EDP_TXP0 48
 28 DDI2_TXN_0 <<< K37 DDI1_TXN[0] EDP_TXN[0] E29 >>> EDP_TXN0 48
 28 DDI2_TXP_1 <<< J35 DDI1_TXP[1] EDP_TXP[1] F28 >>> EDP_TXP1 48
 28 DDI2_TXN_1 <<< J34 DDI1_TXN[1] EDP_TXN[1] E28 >>> EDP_TXN1 48
 28 DDI2_TXP_2 <<< H37 DDI1_TXP[2] EDP_TXP[2] A29 >>> EDP_TXP2 48
 28 DDI2_TXN_2 <<< H36 DDI1_TXN[2] EDP_TXN[2] B29 >>> EDP_TXN2 48
 28 DDI2_TXP_3 <<< J37 DDI1_TXP[3] EDP_TXP[3] C28 >>> EDP_TXP3 48
 28 DDI2_TXN_3 <<< J38 DDI1_TXN[3] EDP_TXN[3] B28 >>> EDP_TXN3 48

28 DDI2_AUXP <<< D27 DDI1_AUXP EDP_AUXP C26 >>> EDP_AUXP 48
 28 DDI2_AUXN <<< E27 DDI1_AUXN EDP_AUXN B26 >>> EDP_AUXN 48

28 DDI1_TXP_0 <<< H34 DDI2_TXP[0] A33 ✕
 28 DDI1_TXN_0 <<< H33 DDI2_TXN[0] D37 >>> DISP_RCOMP
 28 DDI1_TXP_1 <<< F37 DDI2_TXP[1]
 28 DDI1_TXN_1 <<< G38 DDI2_TXN[1]
 28 DDI1_TXP_2 <<< F34 DDI2_TXP[2]
 28 DDI1_TXN_2 <<< F35 DDI2_TXN[2]
 28 DDI1_TXP_3 <<< E37 DDI2_TXP[3]
 28 DDI1_TXN_3 <<< E36 DDI2_TXN[3]

28 DDI1_AUXP <<< F26 DDI2_AUXP
 28 DDI1_AUXN <<< E26 DDI2_AUXN

51 DDI3_TXP_0 <<< C34 DDI3_TXP[0] G27 >>> PROC_AUDIO_CLK 23
 51 DDI3_TXN_0 <<< D34 DDI3_TXN[0] G25 >>> PROC_AUDIO_SDI 23
 51 DDI3_TXP_1 <<< B36 DDI3_TXP[1] G29 >>> PROC_AUDIO_SDO_C 23
 51 DDI3_TXN_1 <<< B34 DDI3_TXN[1] R0801 1 2 20Ohm >>> PROC_AUDIO_SDO 23
 51 DDI3_TXP_2 <<< F33 DDI3_TXP[2]
 51 DDI3_TXN_2 <<< E33 DDI3_TXN[2]
 51 DDI3_TXP_3 <<< C33 DDI3_TXP[3]
 51 DDI3_TXN_3 <<< B33 DDI3_TXN[3]

51 DDI3_AUXP <<< A27 DDI3_AUXP
 51 DDI3_AUXN <<< B27 DDI3_AUXN

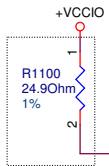
COFFEE LAKE H

Note:
 Trace width=5 mils, Spacing=20mils
 Max length= 600 mils.

Note:
 R0801 close to CPU

+VCCIO
 R0800
 24.9Ohm
 1%
 GND

GPU x 8



Note:
Trace width=5 mils ,Spacing=15mils
Max length= 600 mils.

PEG_RCOMP

20 DMI_RXP0 >>> D8
20 DMI_RXN0 >>> E8
20 DMI_RXP1 >>> F6
20 DMI_RXN1 >>> E6
20 DMI_RXP2 >>> D5
20 DMI_RXN2 >>> E5
20 DMI_RXP3 >>> J8
20 DMI_RXN3 >>> J9

U0800C

E25 D25	PEG_RXP[0] PEG_RXN[0]	PEG_TXP[0] PEG_TXN[0]	B25 A25
E24 F24	PEG_RXP[1] PEG_RXN[1]	PEG_TXP[1] PEG_TXN[1]	B24 C24
E23 D23	PEG_RXP[2] PEG_RXN[2]	PEG_TXP[2] PEG_TXN[2]	B23 A23
E22 F22	PEG_RXP[3] PEG_RXN[3]	PEG_TXP[3] PEG_TXN[3]	B22 C22
E21 D21	PEG_RXP[4] PEG_RXN[4]	PEG_TXP[4] PEG_TXN[4]	B21 A21
E20 F20	PEG_RXP[5] PEG_RXN[5]	PEG_TXP[5] PEG_TXN[5]	B20 C20
E19 D19	PEG_RXP[6] PEG_RXN[6]	PEG_TXP[6] PEG_TXN[6]	B19 A19
E18 F18	PEG_RXP[7] PEG_RXN[7]	PEG_TXP[7] PEG_TXN[7]	B18 C18
D17 E17	PEG_RXP[8] PEG_RXN[8]	PEG_TXP[8] PEG_TXN[8]	A17 B17
F16 E16	PEG_RXP[9] PEG_RXN[9]	PEG_TXP[9] PEG_TXN[9]	C16 B16
D15 E15	PEG_RXP[10] PEG_RXN[10]	PEG_TXP[10] PEG_TXN[10]	A15 B15
F14 E14	PEG_RXP[11] PEG_RXN[11]	PEG_TXP[11] PEG_TXN[11]	C14 B14
D13 E13	PEG_RXP[12] PEG_RXN[12]	PEG_TXP[12] PEG_TXN[12]	A13 B13
F12 E12	PEG_RXP[13] PEG_RXN[13]	PEG_TXP[13] PEG_TXN[13]	C12 B12
D11 E11	PEG_RXP[14] PEG_RXN[14]	PEG_TXP[14] PEG_TXN[14]	A11 B11
F10 E10	PEG_RXP[15] PEG_RXN[15]	PEG_TXP[15] PEG_TXN[15]	C10 B10
G2	PEG_RCOMP		
D8	DMI_RXP[0]	DMI_TXP[0]	B8
E8	DMI_RXN[0]	DMI_TXN[0]	A8
F6	DMI_RXP[1]	DMI_TXP[1]	C6
E6	DMI_RXN[1]	DMI_TXN[1]	B6
D5	DMI_RXP[2]	DMI_TXP[2]	B5
E5	DMI_RXN[2]	DMI_TXN[2]	A5
J8	DMI_RXP[3]	DMI_TXP[3]	D4
J9	DMI_RXN[3]	DMI_TXN[3]	B4

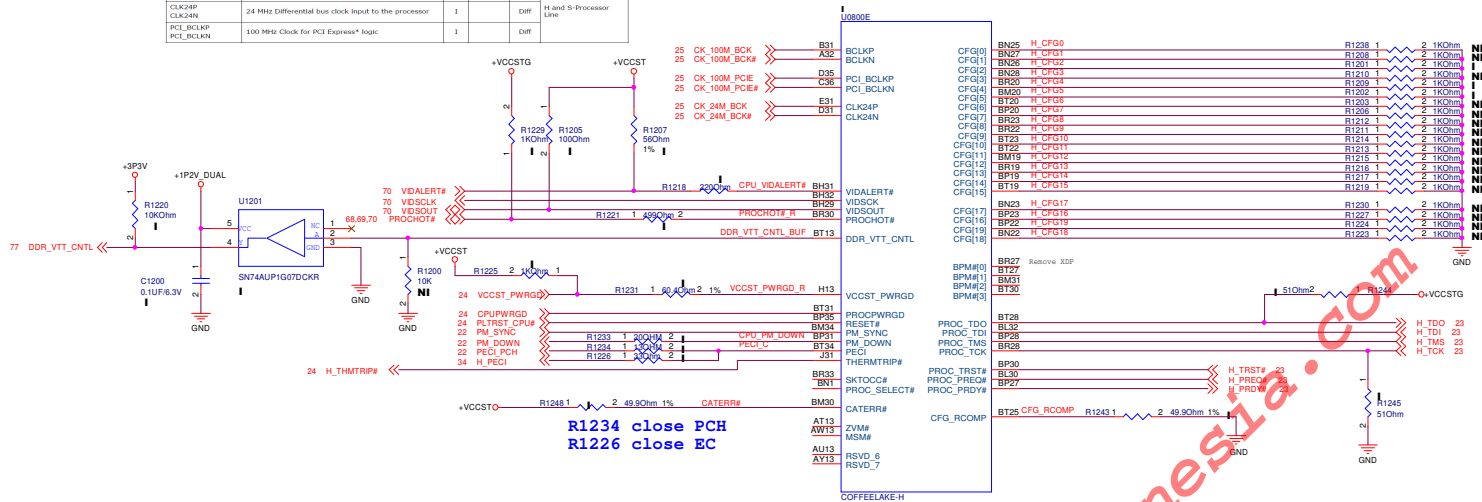
COFFEELAKE-H

A17	EXP_TXP7_C	C1114	2	1	0.22UF/10V	X5R/+/-10%	EXP_TXP7	52
B17	EXP_TXN7_C	C1115	2	1	0.22UF/10V	X5R/+/-10%	EXP_TXN7	52
C16	EXP_TXP6_C	C1112	2	1	0.22UF/10V	X5R/+/-10%	EXP_TXP6	52
B16	EXP_TXN6_C	C1113	2	1	0.22UF/10V	X5R/+/-10%	EXP_TXN6	52
A15	EXP_TXP5_C	C1110	2	1	0.22UF/10V	X5R/+/-10%	EXP_TXP5	52
B15	EXP_TXN5_C	C1111	2	1	0.22UF/10V	X5R/+/-10%	EXP_TXN5	52
C14	EXP_TXP4_C	C1108	2	1	0.22UF/10V	X5R/+/-10%	EXP_TXP4	52
B14	EXP_TXN4_C	C1109	2	1	0.22UF/10V	X5R/+/-10%	EXP_TXN4	52
A13	EXP_TXP3_C	C1106	2	1	0.22UF/10V	X5R/+/-10%	EXP_TXP3	52
B13	EXP_TXN3_C	C1107	2	1	0.22UF/10V	X5R/+/-10%	EXP_TXN3	52
C12	EXP_TXP2_C	C1104	2	1	0.22UF/10V	X5R/+/-10%	EXP_TXP2	52
B12	EXP_TXN2_C	C1105	2	1	0.22UF/10V	X5R/+/-10%	EXP_TXN2	52
A11	EXP_TXP1_C	C1102	2	1	0.22UF/10V	X5R/+/-10%	EXP_TXP1	52
B11	EXP_TXN1_C	C1103	2	1	0.22UF/10V	X5R/+/-10%	EXP_TXN1	52
C10	EXP_TXP0_C	C1100	2	1	0.22UF/10V	X5R/+/-10%	EXP_TXP0	52
B10	EXP_TXN0_C	C1101	2	1	0.22UF/10V	X5R/+/-10%	EXP_TXN0	52

GPU x 8

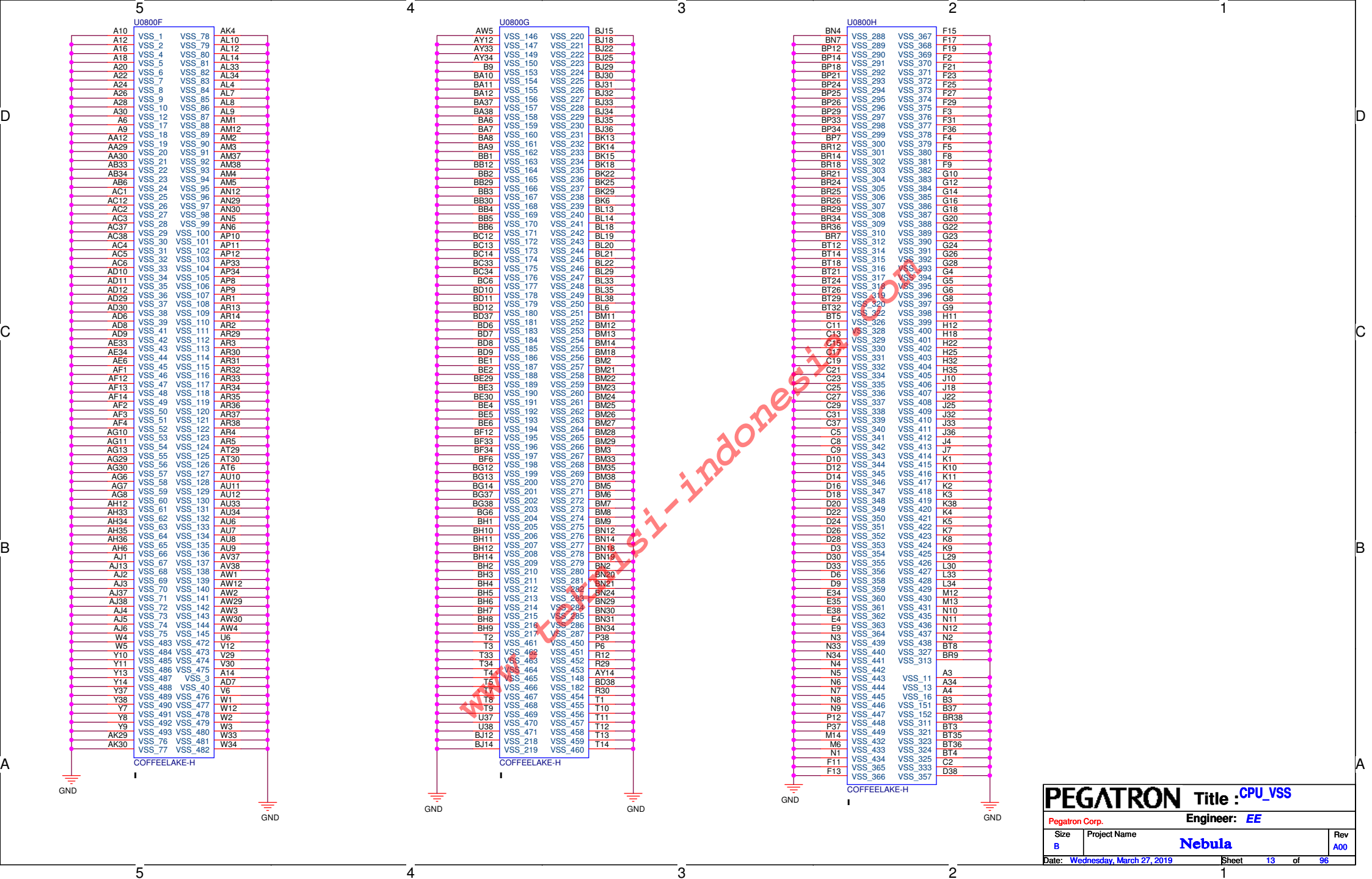
PEGATRON		Title : CPU_DMI/PEG	
Pegatron Corp.		Engineer: EE	
Size B	Project Name Nebula	Rev A00	
Date: Wednesday, March 27, 2019		Sheet 11 of 96	

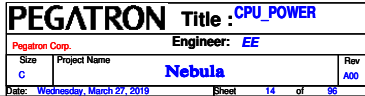
Signal Name	Description	Dir.	Buffer Type	Link Type	Availability
BCLKP BCLKN	100 MHz Differential bus clock input to the processor	I		Diff	H and S-Processor Line
CLK24P CLK24N	24 MHz Differential bus clock input to the processor	I		DIFF	
PCI_BCLKP PCI_BCLKN	100 Mhz Clock for PCI Express* logic	I		Diff	

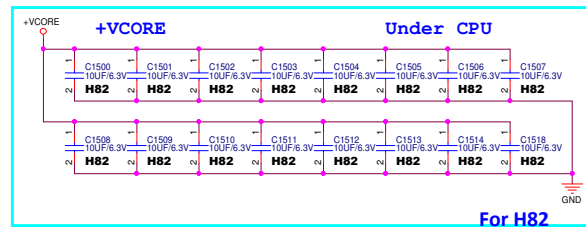


Signal Name	Description
CFG[19:0]	<p>Configuration Signals: The CFG signals have a default value of '1' if not terminated on the board. Refer to the appropriate platform design guide for pull-down recommendations when a logic low is desired.</p> <p>Intel recommends placing test points on the board for CFG pins.</p> <ul style="list-style-type: none"> • CFG[0]: Stall reset sequence after PCU PLL lock until de-asserted: <ul style="list-style-type: none"> — 1 = (Default) Normal Operation; No stall. — 0 = Stall. • CFG[1]: Reserved configuration lane. • CFG[2]: PCI Express* Static x16 Lane Numbering Reversal. <ul style="list-style-type: none"> — 1 = Normal operation — 0 = Lane numbers reversed. • CFG[3]: Reserved configuration lane. • CFG[4]: eDP enable: <ul style="list-style-type: none"> — 1 = Disabled. — 0 = Enabled. • CFG[6:5]: PCI Express* Bifurcation <ul style="list-style-type: none"> — 00 = 1 x8, 2 x4 PCI Express* — 01 = reserved — 10 = 2 x8 PCI Express* — 11 = 1 x16 PCI Express* • CFG[7]: PEG Training: <ul style="list-style-type: none"> — 1 = (default) PEG Train immediately following RESET# de assertion. — 0 = PEG Wait for BIOS for training. • CFG[19:8]: Reserved configuration lanes.

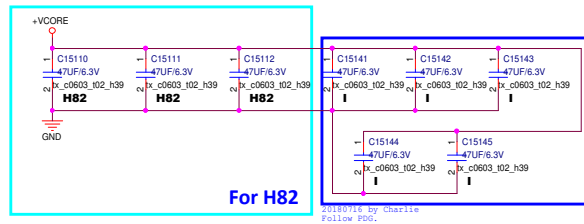
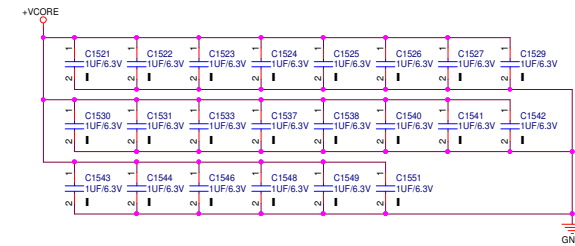
Pin Name	Strap Description	Configuration (Default Value for Each Bit is 1 Unless Specified)	Default Value	✓
CFG[19:8]	Reserved configuration lands.			







For H82
20180716 by Charlie
Change to H82.



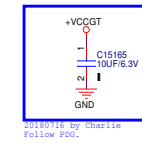
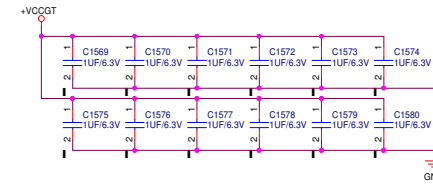
For H82

20180716 by Charlie
Follow P00.

Table 50-3. Decoupling Requirements for CFL H Processor

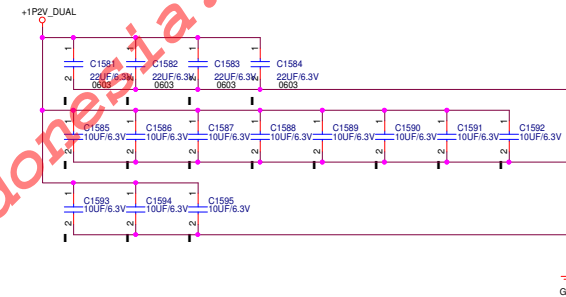
Domain	Board Edge cap	Backside cap	Notes
Vcc	5x 47uF 0805	12x 22uF 0603	Place as close to the BGA as possible
		21x 10uF 0402	
		24x 1uF 0201	
		24x 0201 (placeholder)	
VccGT	3x 47uF 0805	10x 10uF 0402	
	7x 22uF 0603	12x 1uF 0201	
VccSA	2x 47uF 0805	7x 10uF 0402	
	2x 22uF 0603	1x 1uF 0201	
VDDQ		4x 22uF 0603	
		11x 10uF 0402	
VccIO		3x 10uF 0402	Additional capacitors might be needed if the connectivity from BGA to capacitors is not adequate.
		3x 0402 (placeholder)	

+VCCGT Under CPU

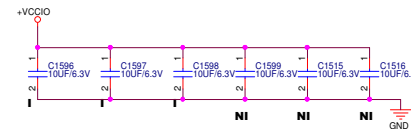


20180716 by Charlie
Follow P00.

+1P2V_DUAL Under CPU



+VCCIO Under CPU



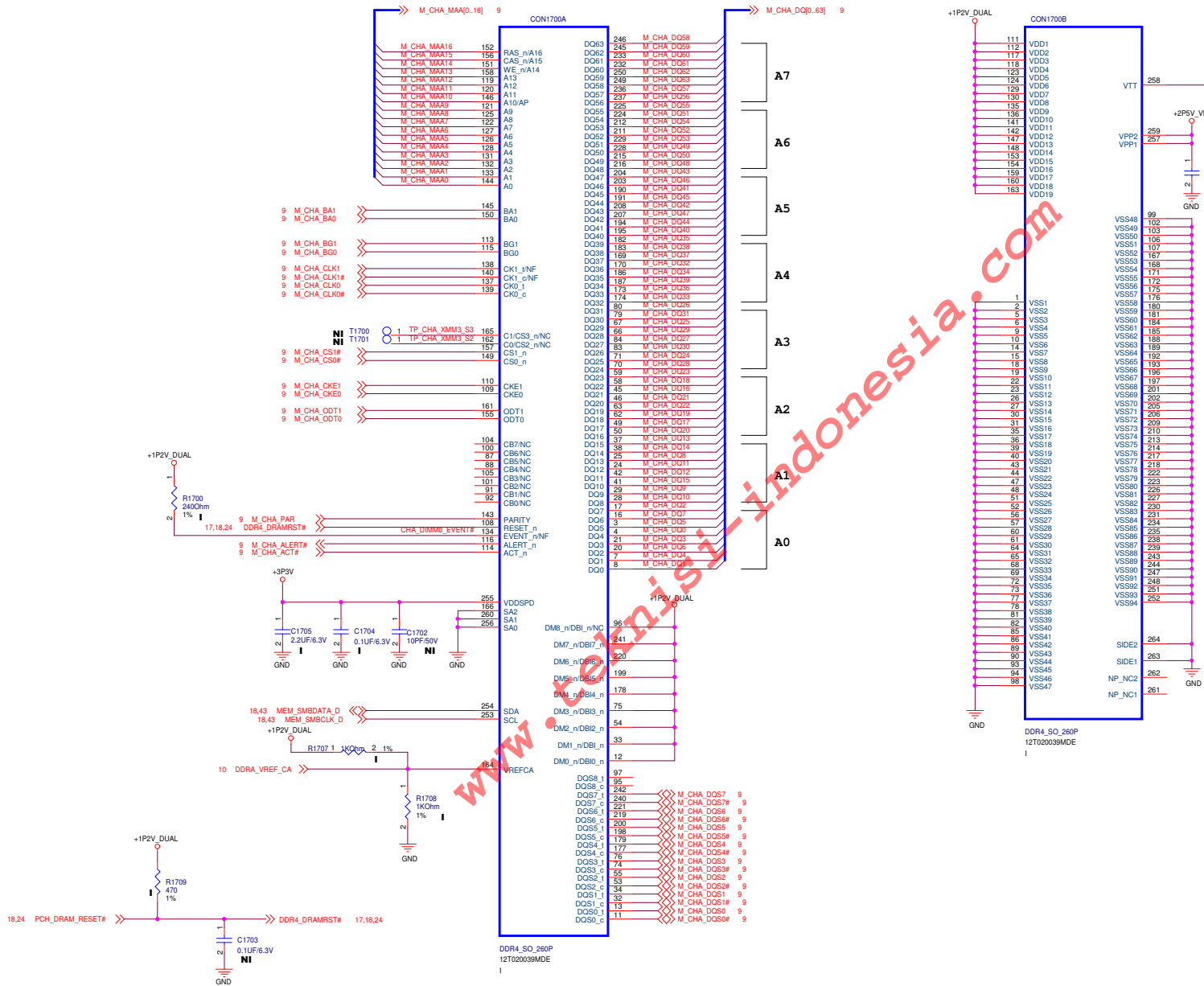
+VCCSA Under CPU



Reserve Page

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PEGATRON		Title : XXX	
Pegatron Corp.		Engineer: EE	
Size B	Project Name Nebula		Rev A00
Date: Wednesday, March 27, 2019		Sheet	16 of 96

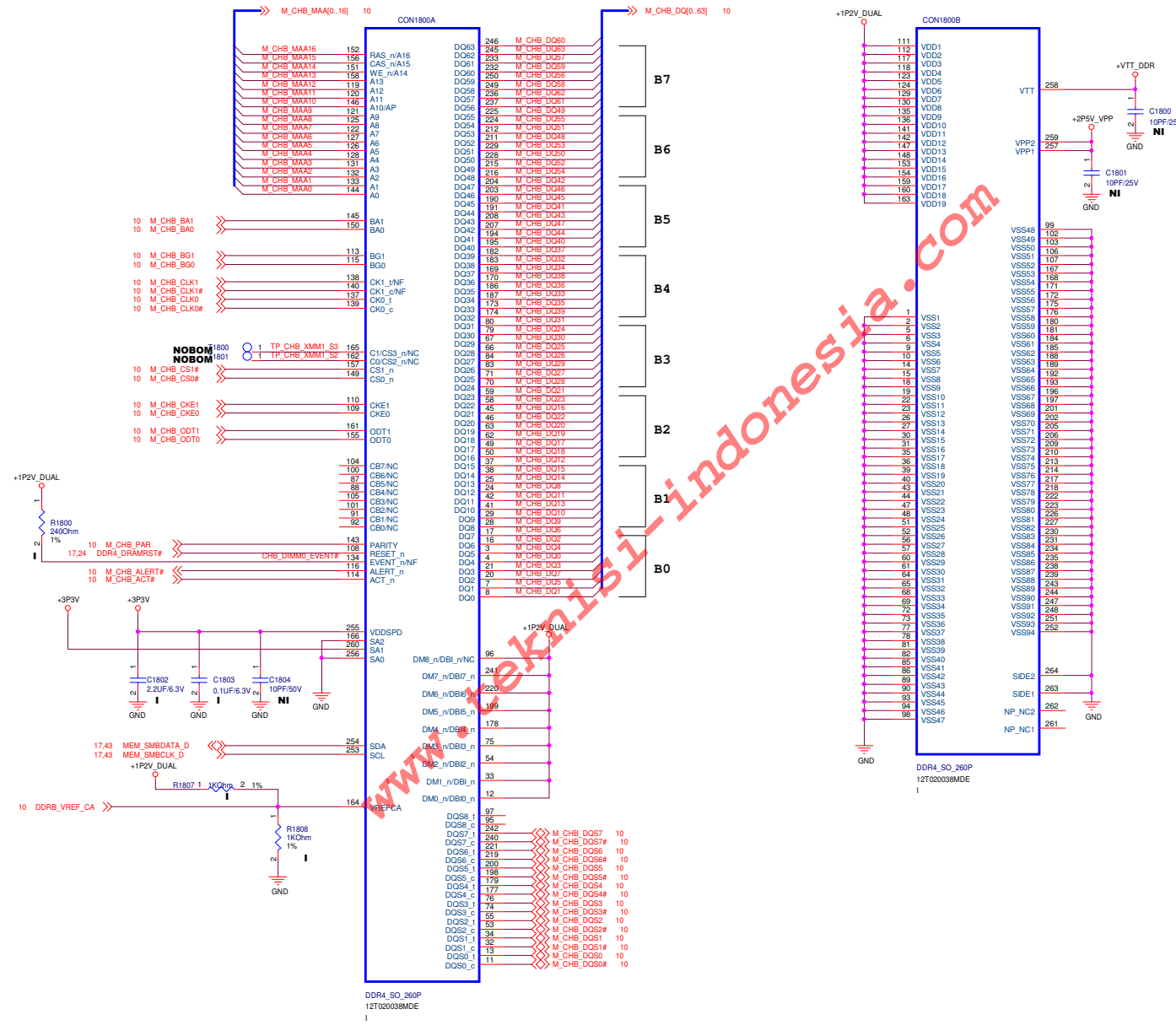


PEGATRON Title: **DDR4 SO-DIMM**

Pegatron Corp. Engineer: **EE**

Size: **C** Project Name: **Nebula** Rev: **A00**

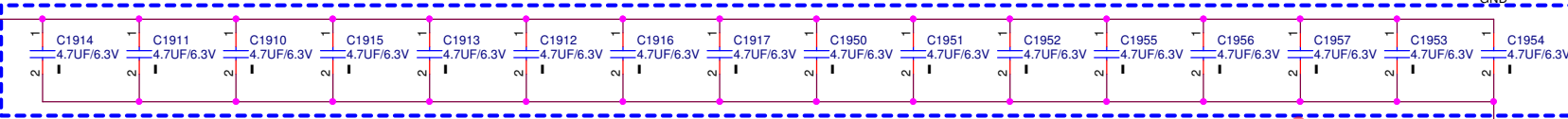
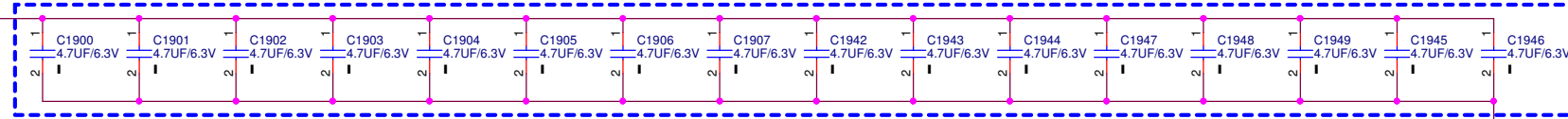
Date: **Wednesday, March 27, 2019** Sheet: **17** of **95**



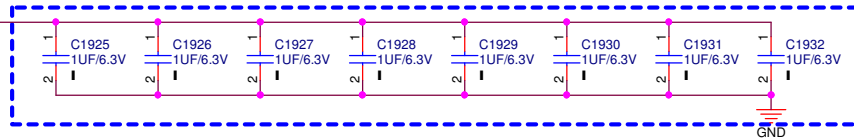
+1P2V_DUAL

Change all 10u to 4.7u*2 for placement - 2017-1/4

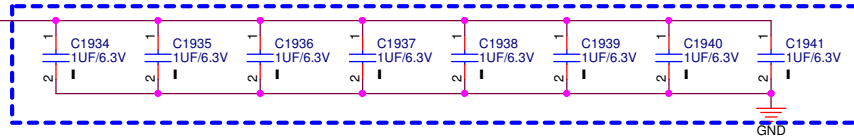
close
CH A SO-DIMM



close
CH B SO-DIMM



close
CH A SO-DIMM



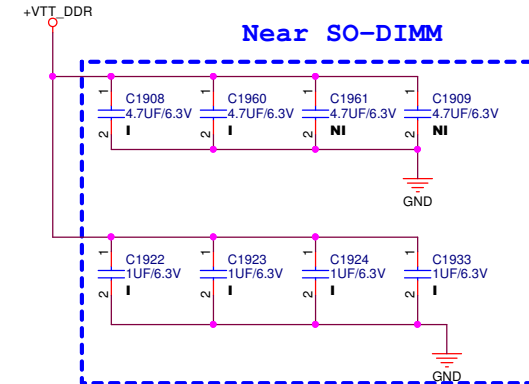
close
CH B SO-DIMM

Change all 1uF from 0402 package to 0201 for placement - 2017-1/4

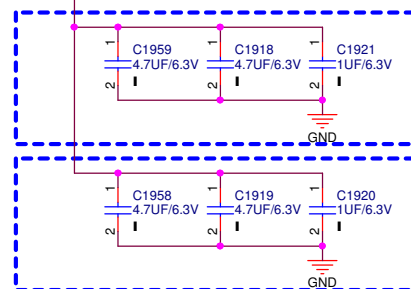
DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)	Note
DDR4 2 Channels SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10 μ F (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1 μ F (0402)	
		1 placeholder	1x 330 μ F (7343)	
	VTT	Place these caps on the VTT plane close to SODIMM	1x 10 μ F (0603)	
		Placeholder	1x 10 μ F (0603)	
		Place these caps on the VTT plane close to SODIMM	4x 1 μ F (0402)	
	VPP	DRAM Side	2x 10 μ F (0603)	
		DRAM Side	2x 1 μ F (0402)	
	VDDSPD	Place close to DIMM	1x 0.1 μ F (0402)	
		Place close to DIMM	1x 2.2 μ F (0402)	

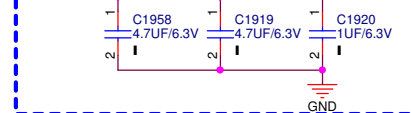
Near SO-DIMM



+2P5V_VPP

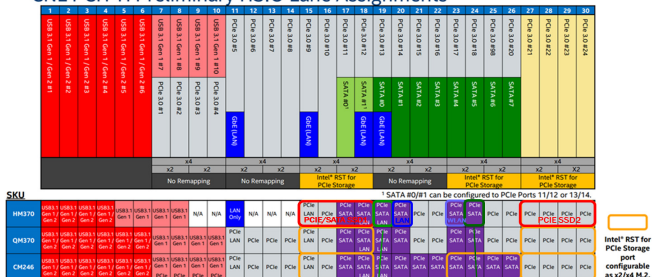


close CH A SO-DIMM

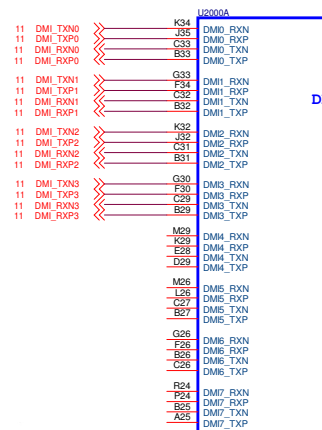
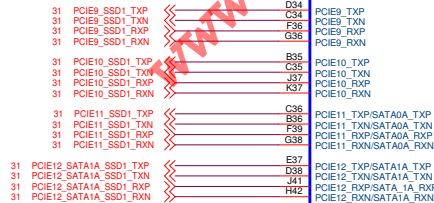


close CH B SO-DIMM

CNL PCH-H Preliminary HSIO Lane Assignments



M.2 PCIe X4 #1



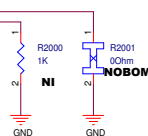
DMI

USB2.0

PCIE/USB/SATA

USB3.1

USB ID
USB2_VBUSSENSE



PEGATRON Title : PCH_DMI_PCIE_USB_SATA_1-8

Pegatron Corp.		Engineer: EE	
Size	Project Name	Rev	
C	Nebula	A00	
Date: Wednesday, March 27, 2019		Sheet	20 of 95

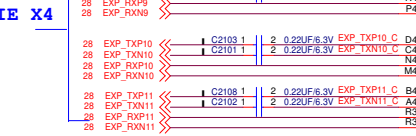
HDD



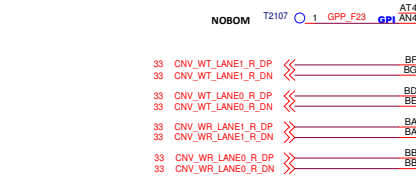
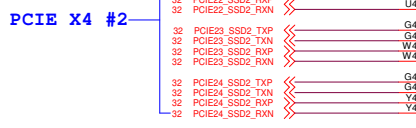
M.2 KEY-E WLAN



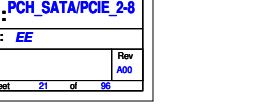
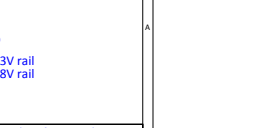
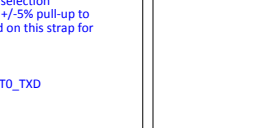
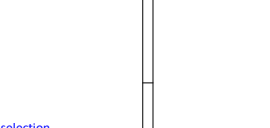
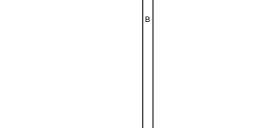
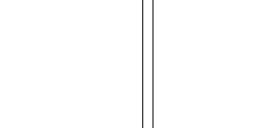
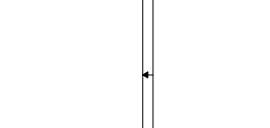
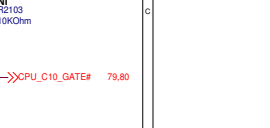
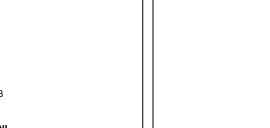
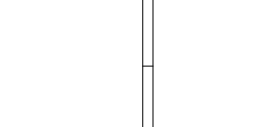
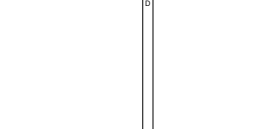
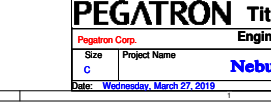
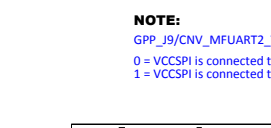
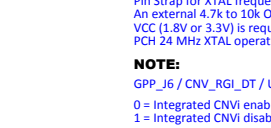
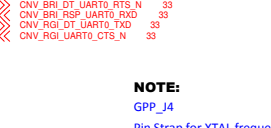
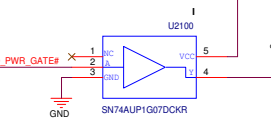
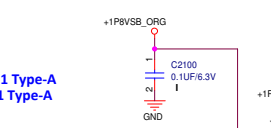
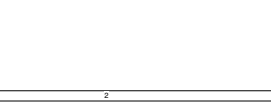
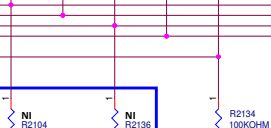
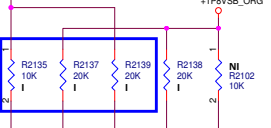
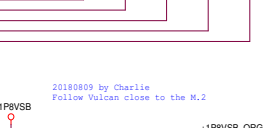
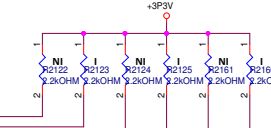
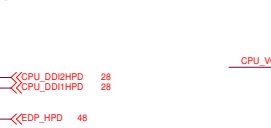
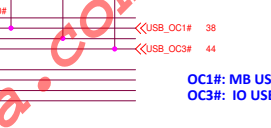
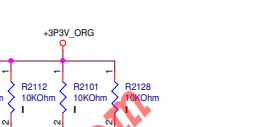
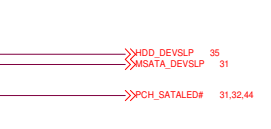
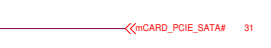
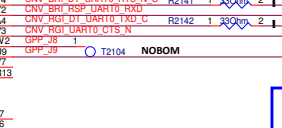
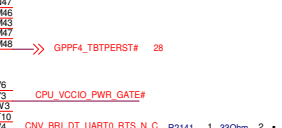
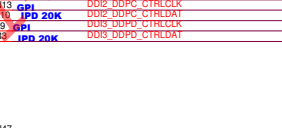
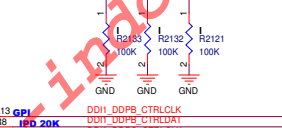
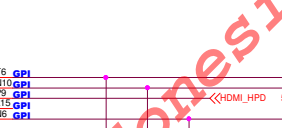
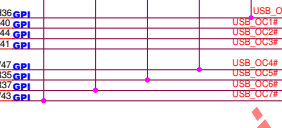
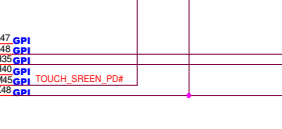
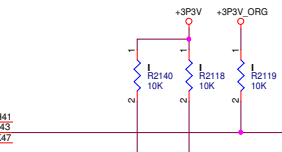
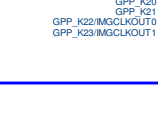
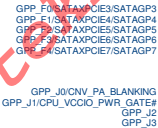
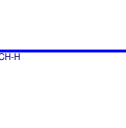
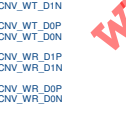
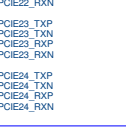
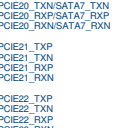
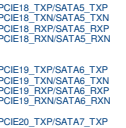
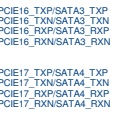
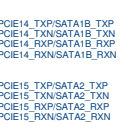
Alpine Ridge PCIe X4



M.2 PCIe X4 #2



PCIe/SATA



NOTE:
GPP_J4
Pin Strap for XTAL frequency selection
An external 4.7k to 10k Ohm +/-5% pull-up to VCC (1.8V or 3.3V) is required on this strap for PCH 24 MHz XTAL operation

NOTE:
GPP_J6 / CNV_RGI_DT / UART0_TXD
0 = Integrated CNVI enable.
1 = Integrated CNVI disable.

NOTE:
GPP_J9/CNV_MFUART2_TXD
0 = VCCSPI is connected to 3.3V rail
1 = VCCSPI is connected to 1.8V rail

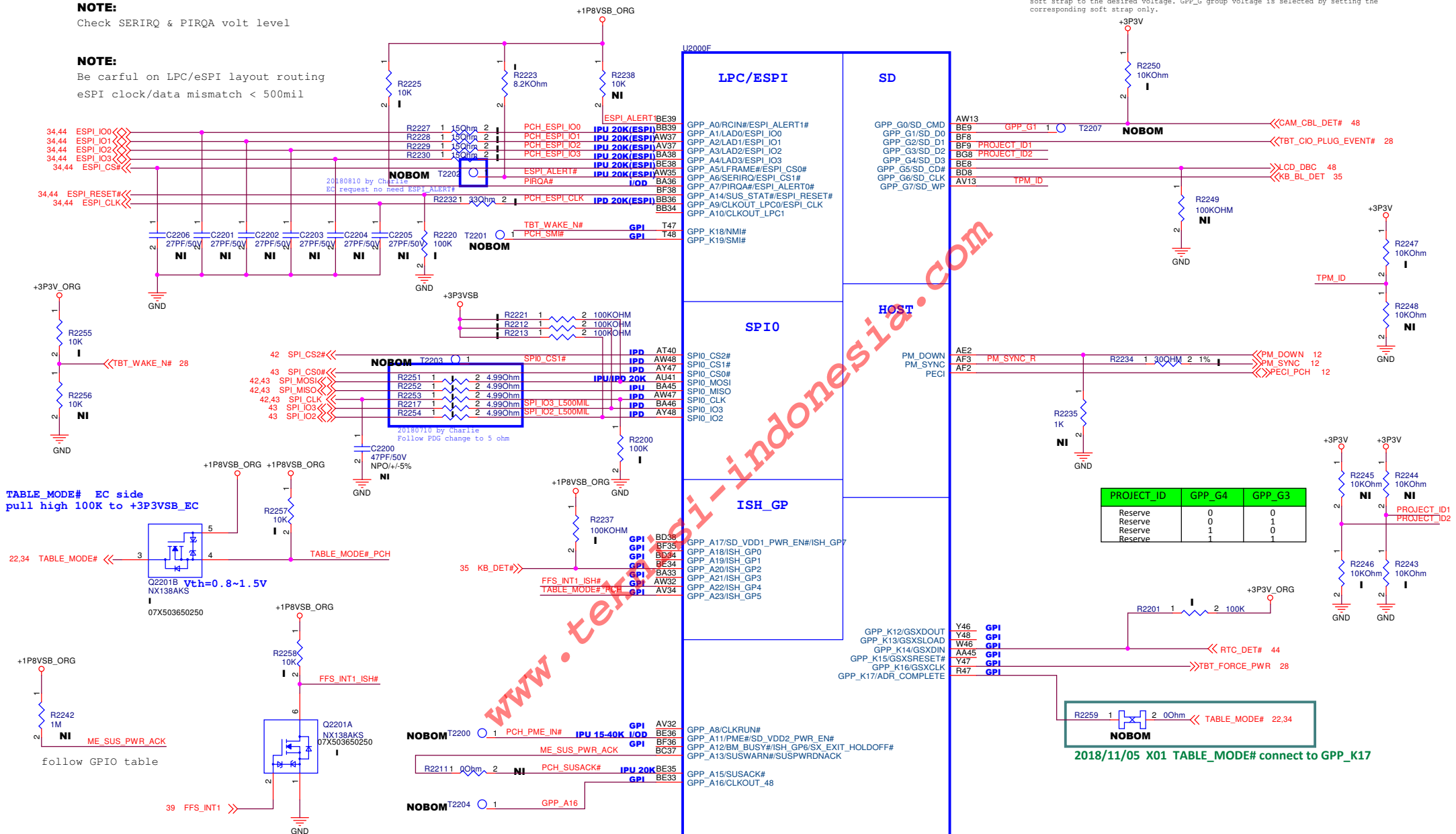
eSPI operates at 1.8V

Check SERIRQ & PIRQA volt level

Be careful on LPC/eSPI layout routing
eSPI clock/data mismatch < 500mil

Check GPP_A0 power well

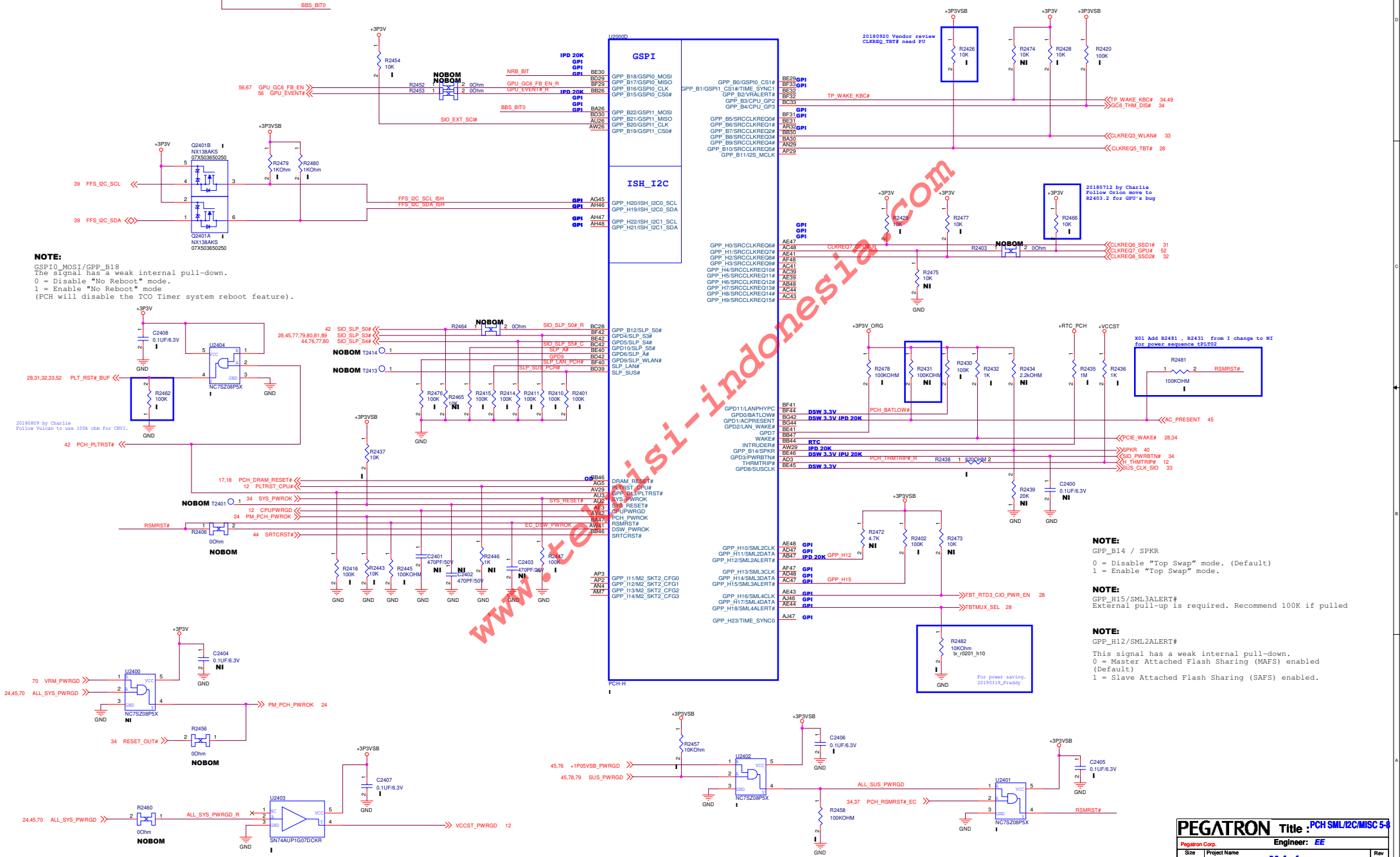
GPP_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltageselection soft strap to the desired voltage. GPP_G group voltage is selected by setting the corresponding soft strap only.



If Deep Sx is supported, the EC/motherboard controlling logic must change SUSACK# to match SUSWARN# once the EC/motherboard controlling logic has completed the preparations discussed in the description for the SUSWARN# pin.

Pegatron Corp.		Engineer: EE	
Size Custom	Project Name Nebula	Rev A00	
Date: <u>Wednesday, March 27, 2019</u>		Sheet <u>22</u> of <u>96</u>	

NOTE:
GPP_B22/GSPI1_MOSI
This signal has a weak internal pull-down.
Offset 3410h:Bit 10
0: SPI
1: LPC



NOTE:
GSPi0_MOSI/GPP_B18
The signal has a weak internal pull-down.
0 = Disable "No Reboot" mode.
1 = Enable "No Reboot" mode
(PCH will disable the TCO Timer system reboot feature).

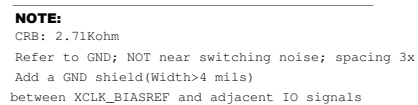
20180809 by Charlie
Follow Vulcan to use 100k ohm for CPU7.

20180920 Vendor review
CLEARB2_TBT# need PO

NOTE:
GPP_B14 / SPKR
0 = Disable "Top Swap" mode. (Default)
1 = Enable "Top Swap" mode.

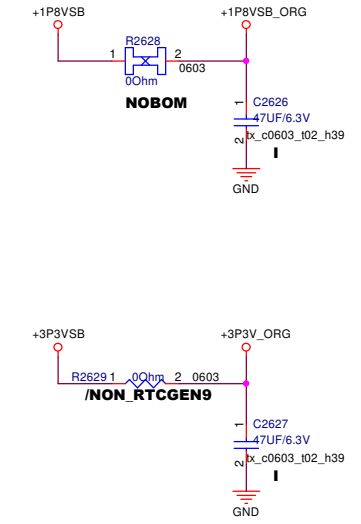
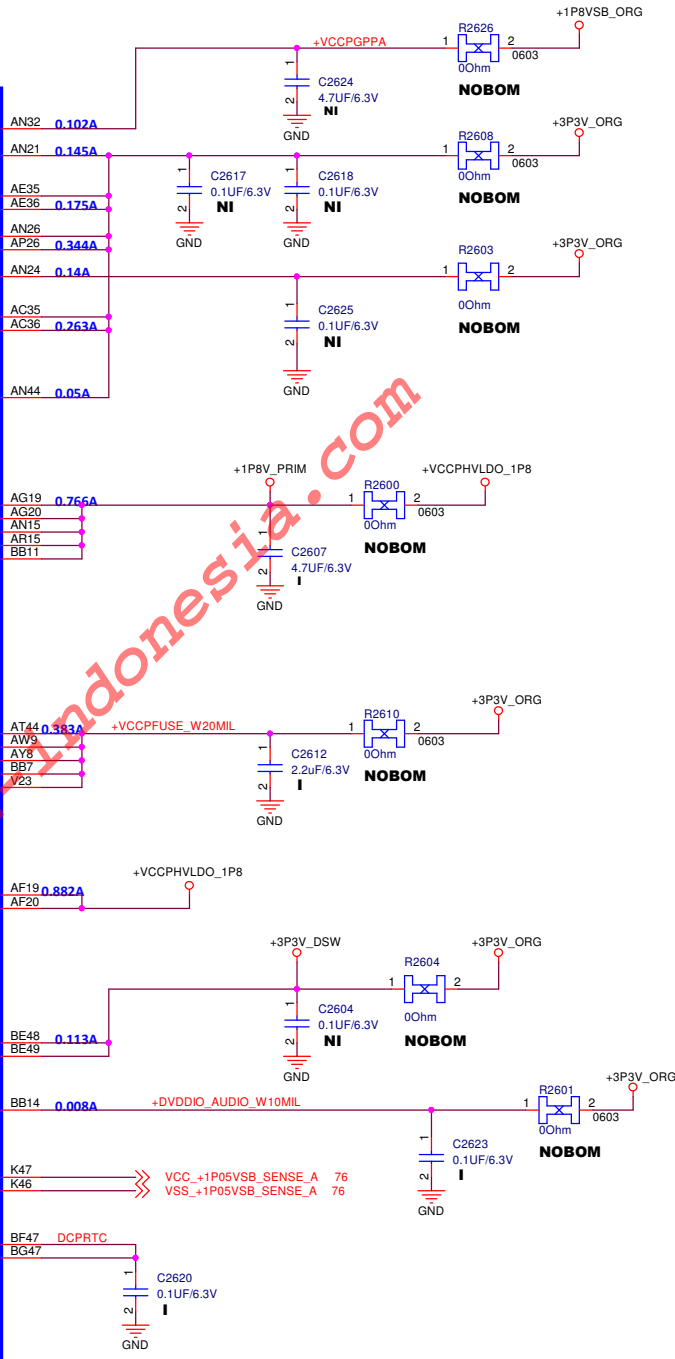
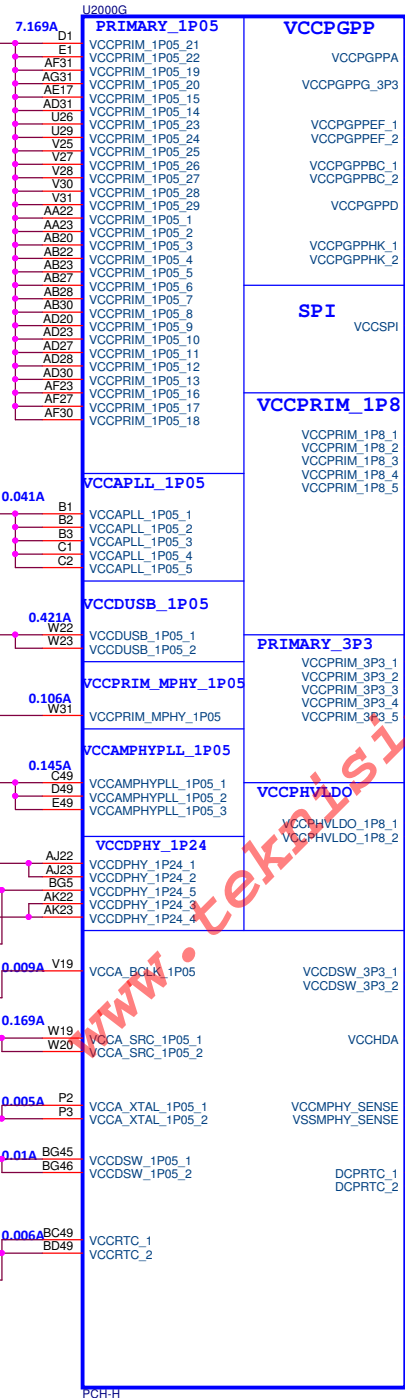
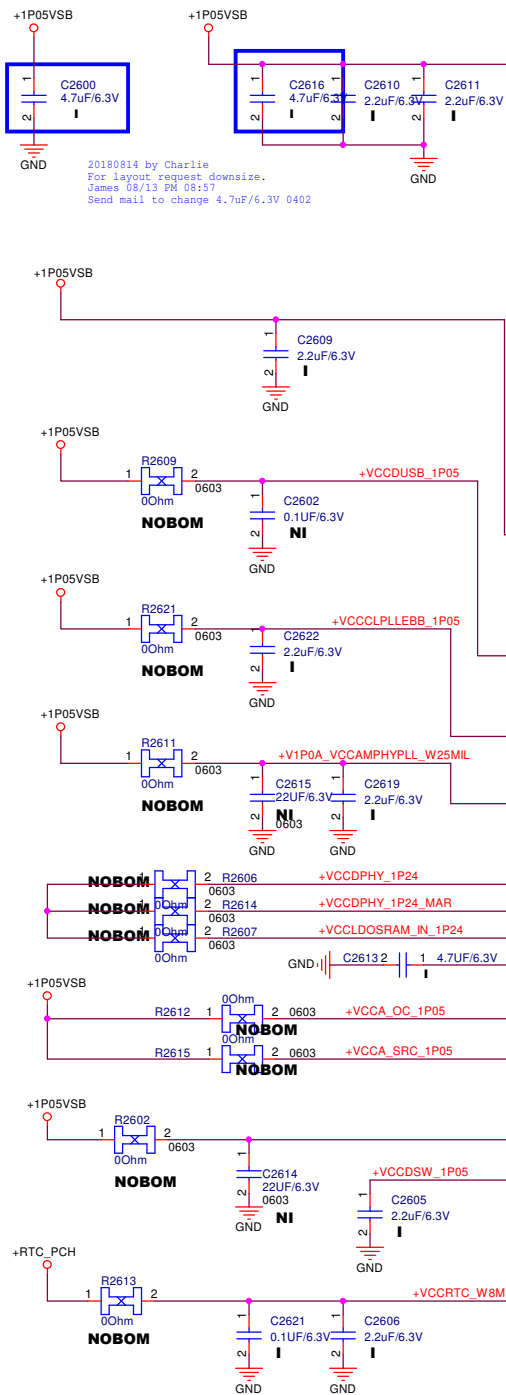
NOTE:
GPP_H15/SML3ALERT#
External pull-up is required. Recommend 100K if pulled

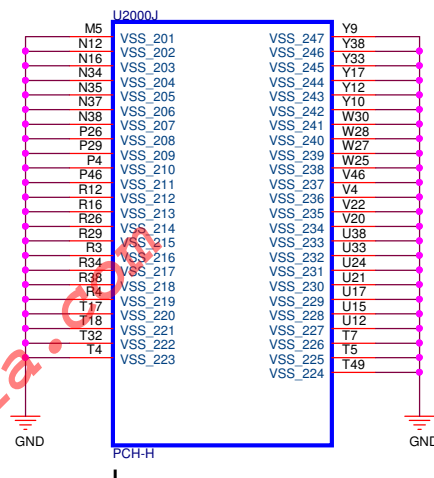
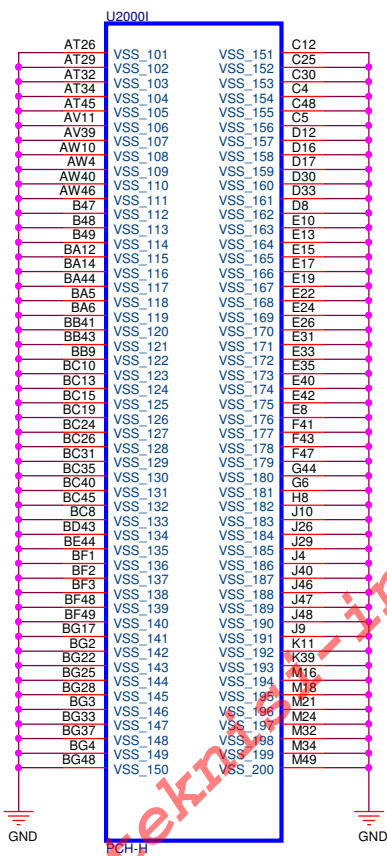
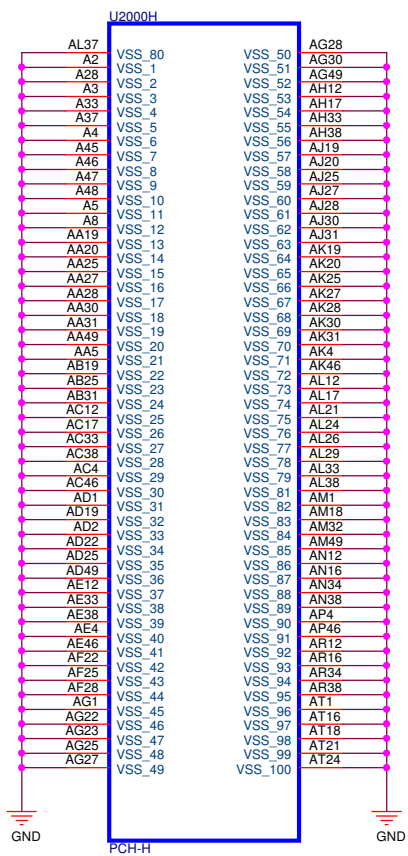
NOTE:
GPP_H12/SML2ALERT#
This signal has a weak internal pull-down.
0 = Master Attached Flash Sharing (MAFS) enabled
(Default)
1 = Slave Attached Flash Sharing (SAFS) enabled.

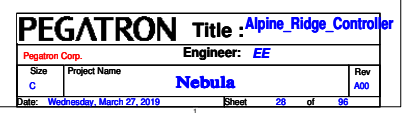


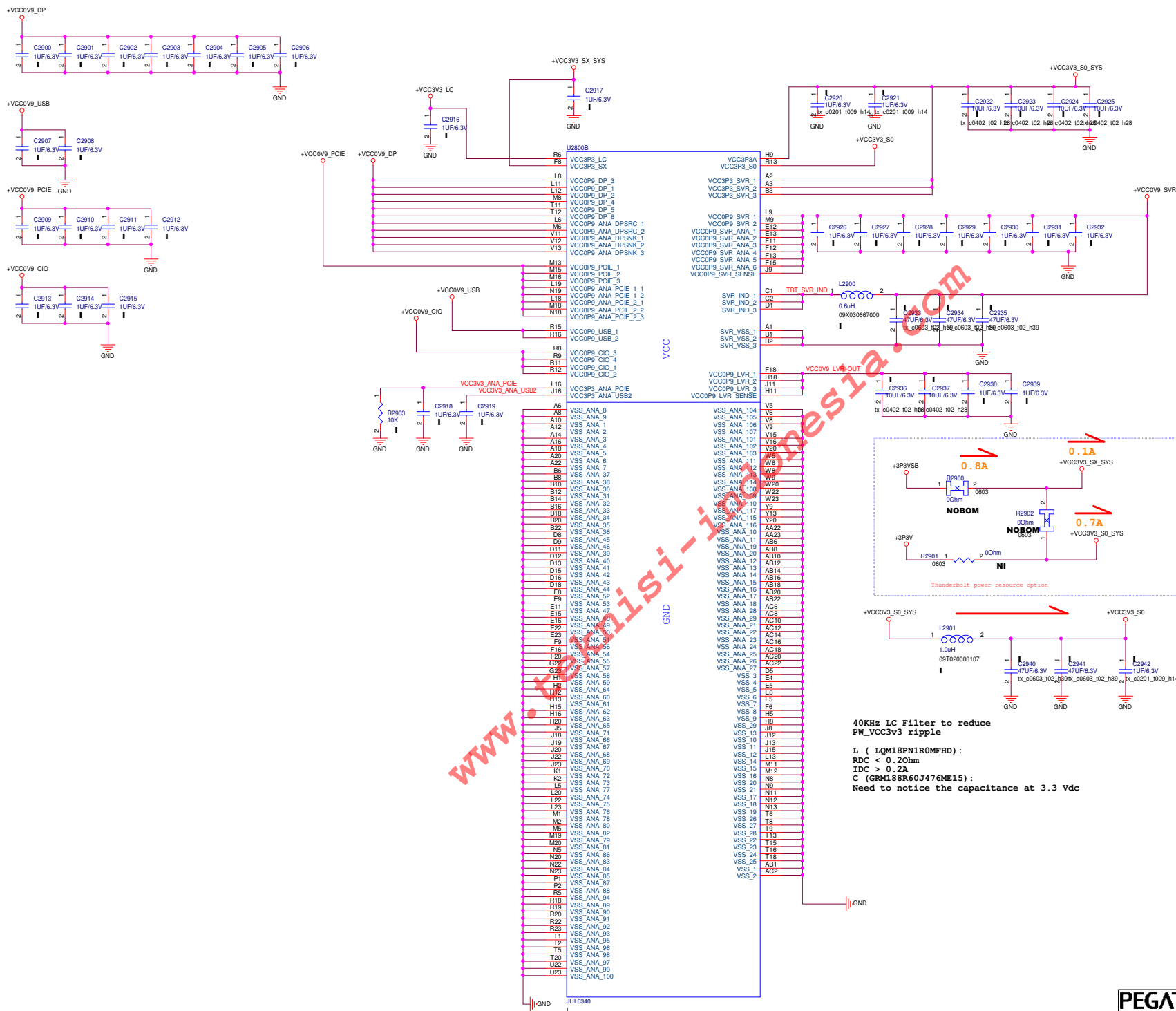
Parameter	Values	Units	Max/Min Range
Frequency	24	MHz	
Frequency Tolerance	± 100	PPM	
Duty Cycle Variation	+/- 5	%	
Pk to Pk Jitter	± 150	pS	Includes cycle to cycle and period to period jitter
Operating Temperature	-40 to 85	°C	
Series Resistance	± 30	Ω	
Aging	± 3	PPM	

NOTE:
24MHz crystal : ESR 30 OHM









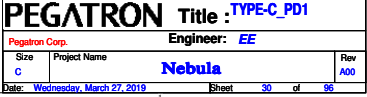
40KHz LC Filter to reduce
PW_VCC3V3 ripple
L (LQM18PNIROMFHD) :
RDC < 0.20hm
IDC > 0.2A
C (GRM188R60J476ME15) :
Need to notice the capacitance at 3.3 Vdc

PEGATRON Title : Alpine Ridge Power

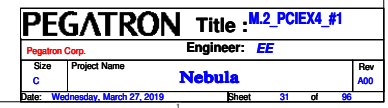
Pegatron Corp. Engineer: EE

Size Project Name Nebula Rev A00

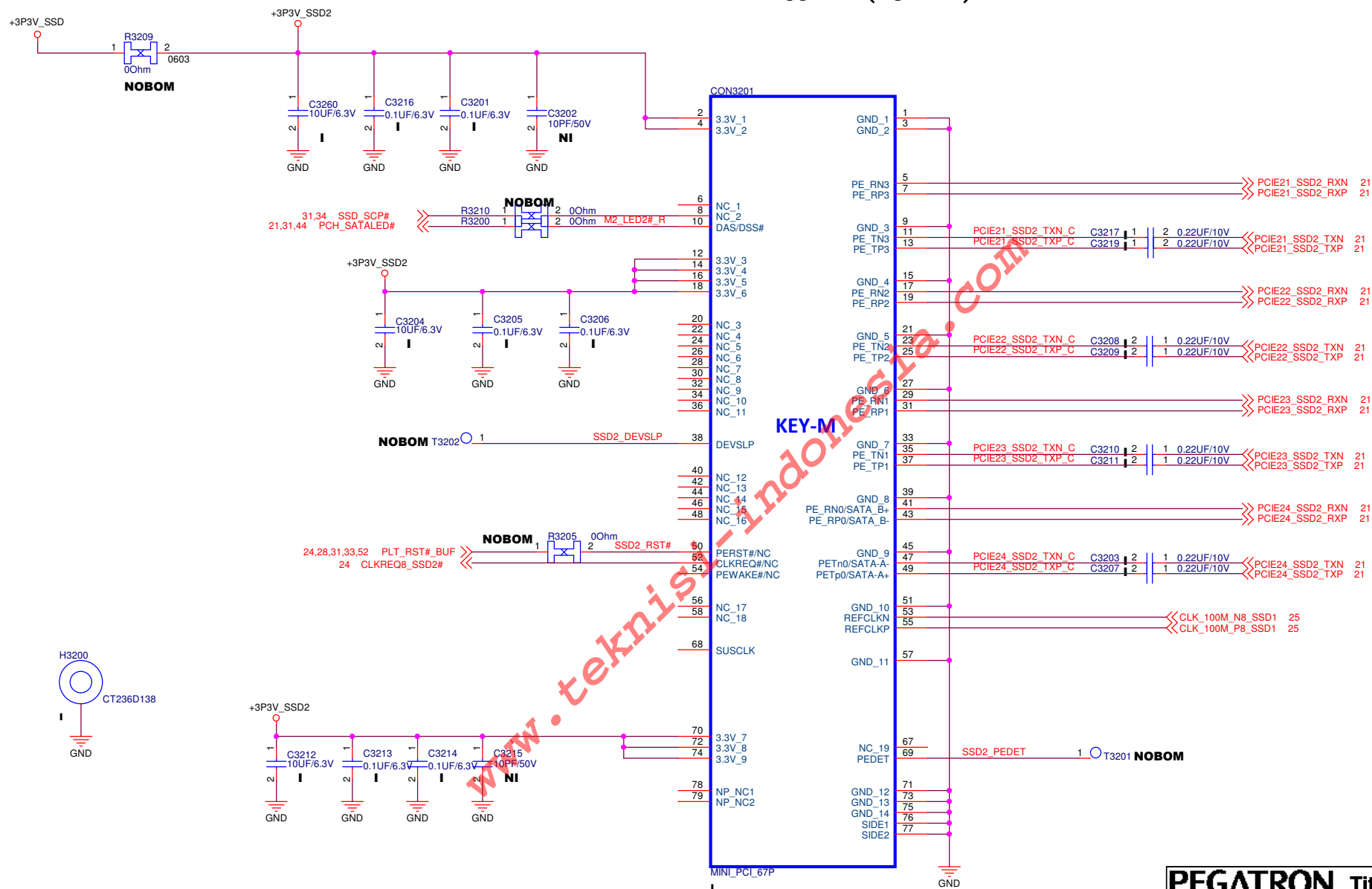
Date: Wednesday, March 27, 2019 Sheet 29 of 95



PCIE/SATA SSD by BOM change 0.1uF/0.22uF



M.2 KEY-M SSD #1 (PCIe x4)



PEGATRON Title : **M.2_PCIEX4_#2**

Pegatron Corp.		Engineer: EE	
Size B	Project Name Nebula	Rev A00	
Date: Wednesday, March 27, 2019		Sheet 32	of 96

[illegible]

M.2 KEY-E WLAN

The diagram illustrates the M.2 KEY-E WLAN connection for a Raspberry Pi 4B. It shows the connection between the M.2 connector pins (78 and 79) and the internal components of the Pi 4B, including the USB14_R and USB14_RN ports, the L3300 90ohm inductor, and the RN3313B and RN3313A components. The diagram also shows the connection to the USB14_R and USB14_RN ports.

Pin 78 (NP_NC1 / SIDE1):

- 1: 1
- 2: 2
- 3: 3
- 4: 4
- 5: 5
- 6: 6
- 7: 7
- 8: 8
- 9: 9
- 10: 10
- 11: 11
- 12: 12
- 13: 13
- 14: 14
- 15: 15
- 16: 16
- 17: 17
- 18: 18
- 19: 19
- 20: 20
- 21: 21
- 22: 22
- 23: 23
- 24: 24
- 25: 25
- 26: 26
- 27: 27
- 28: 28
- 29: 29
- 30: 30
- 31: 31
- 32: 32
- 33: 33
- 34: 34
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- 36: 36
- 37: 37
- 38: 38
- 39: 39
- 40: 40
- 41: 41
- 42: 42
- 43: 43
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- 46: 46
- 47: 47
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- 51: 51
- 52: 52
- 53: 53
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- 56: 56
- 57: 57
- 58: 58
- 59: 59
- 60: 60
- 61: 61
- 62: 62
- 63: 63
- 64: 64
- 65: 65
- 66: 66
- 67: 67
- 68: 68
- 69: 69
- 70: 70
- 71: 71
- 72: 72
- 73: 73
- 74: 74
- 75: 75
- 76: 76
- 77: 77
- 78: 78
- 79: 79

Pin 79 (NP_NC2 / SIDE2):

- 1: 1
- 2: 2
- 3: 3
- 4: 4
- 5: 5
- 6: 6
- 7: 7
- 8: 8
- 9: 9
- 10: 10
- 11: 11
- 12: 12
- 13: 13
- 14: 14
- 15: 15
- 16: 16
- 17: 17
- 18: 18
- 19: 19
- 20: 20
- 21: 21
- 22: 22
- 23: 23
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- 25: 25
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- 27: 27
- 28: 28
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- 31: 31
- 32: 32
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- 65: 65
- 66: 66
- 67: 67
- 68: 68
- 69: 69
- 70: 70
- 71: 71
- 72: 72
- 73: 73
- 74: 74
- 75: 75
- 76: 76
- 77: 77
- 78: 78
- 79: 79

Internal Components:

- CON3300
- NP_NC1
- SIDE1
- NP_NC2
- SIDE2
- MINI_100_67P
- USB14_R
- USB14_RN
- L3300 90ohm
- RN3313B
- RN3313A
- USB14_R
- USB14_RN

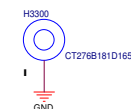
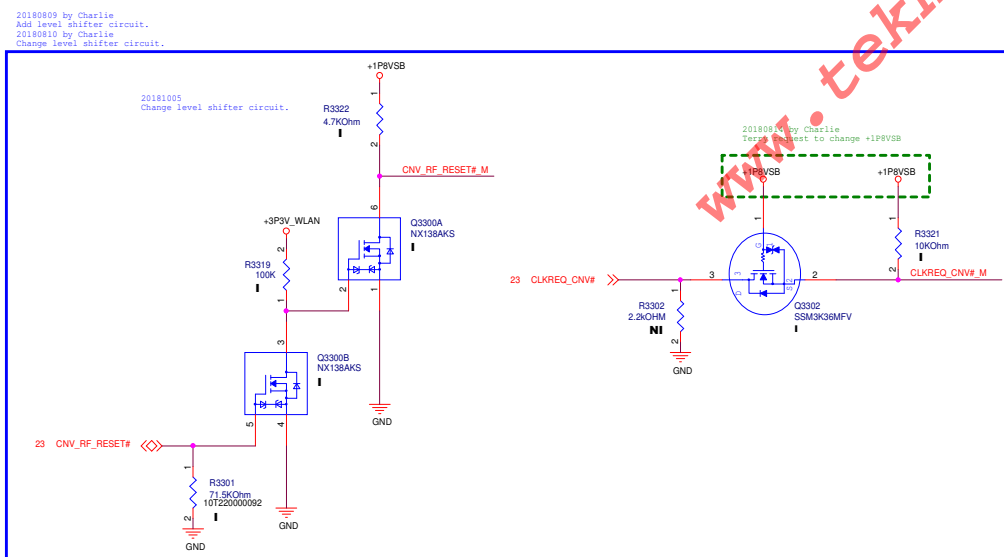
Notes:

- Change to use 0.1uF 0201.
- CS307 2 1 0.1uF 6.3V
- CS308 2 1 0.1uF 6.3V
- CS307 2 1 0.1uF 6.3V
- CS308 2 1 0.1uF 6.3V

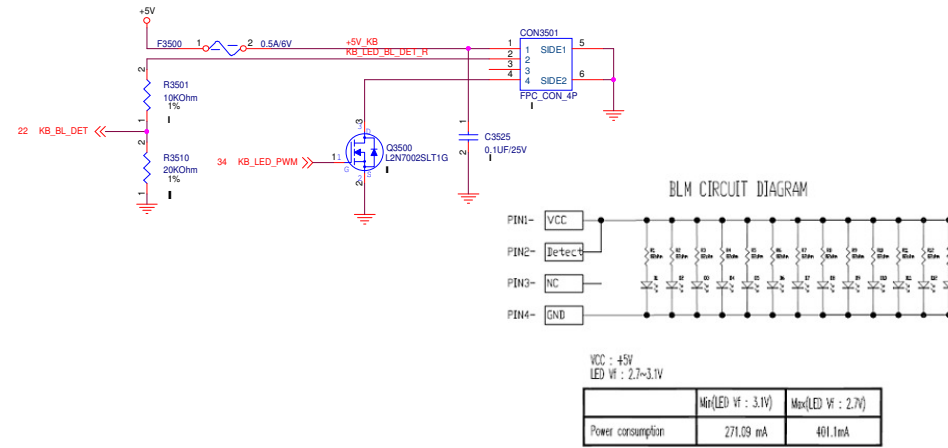
```

Remark: 1.NC is not connected; YES is connected.
2. Pin54 is BT_DISABLE; Pin56
3. Pin 20,22,32,34 and 36 are GPIO and have internal pull up(QCA6174A25), Suggest
platform NC those pins.
4. Pin44, 46, 48, QCA suggest platform to NC.
5. Pin17 and 19 suggest reserve test point at platform side.

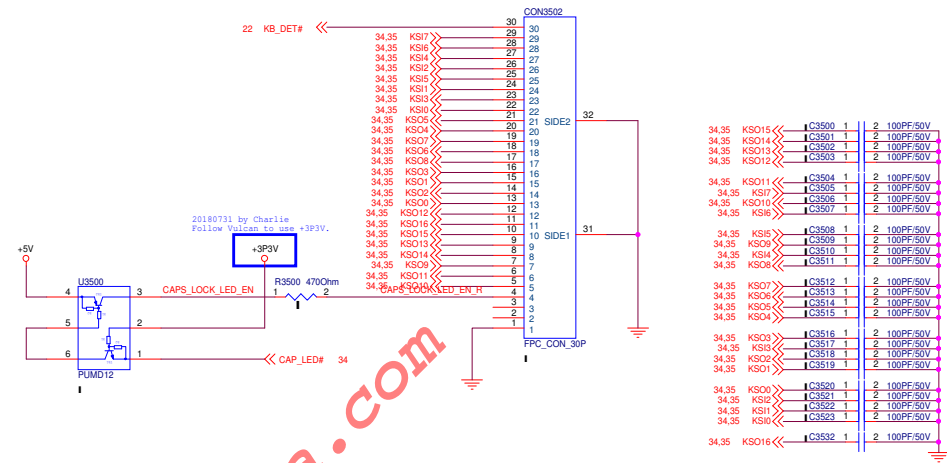
```



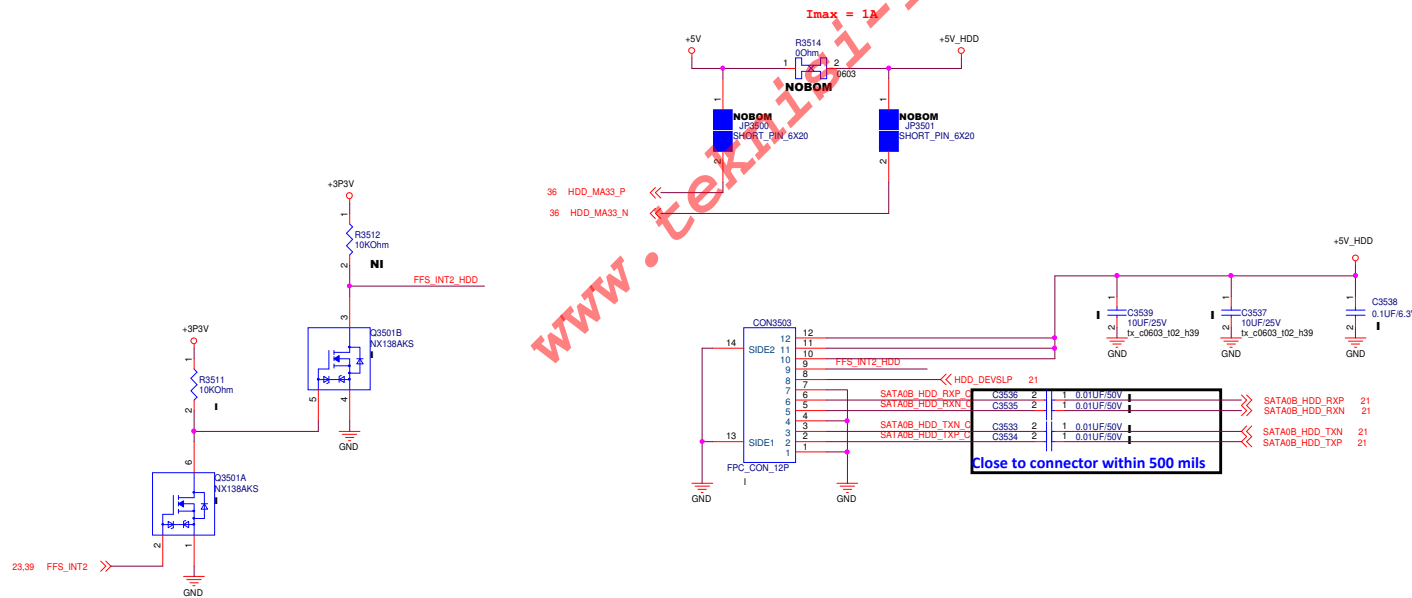
KB BL Conn



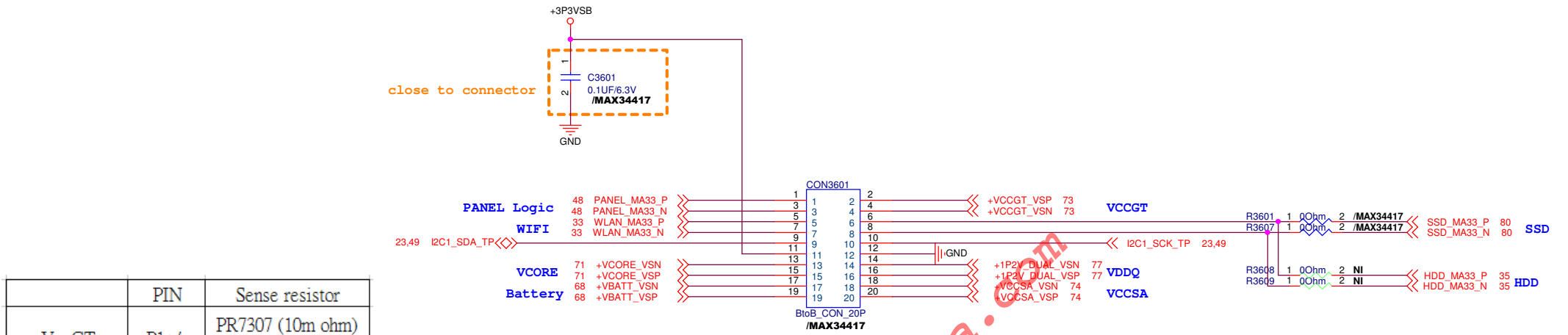
KB Conn



SATA HDD



POWER SENSE MAX34417



	PIN	Sense resistor
VccGT	P1+/-	PR7307 (10m ohm) PR7308 (10m ohm)
SSD	P2+/-	R4852 (10m ohm)
HDD(SATA)		R3126 (10m ohm)
WIFI	P3+/-	R3313 (10m ohm)
Panel logic	P4+/-	R3109 (10m ohm)
Battery	P5+/-	R6811 (5m ohm)
Vcore	P6+/-	PR7100 (10m ohm)
		PR7101 (10m ohm)
VDDQ	P7+/-	PR7700 (10m ohm)
VccSA	P8+/-	PR7407 (10m ohm)

2	4	6	8	10	12	14	16	18	20
P1+	P1-	P2+	P2-	CLK	GND	P7-	P7+	P8-	P8+
P4+	P4-	P3+	P3-	DATA	3.3V	P6-	P6+	P5-	P5+
1	3	5	7	9	11	13	15	17	19

PEGATRON

Title : POWER_SENSE_MAX34417

Pegatron Corp.

Engineer: EE

Size B

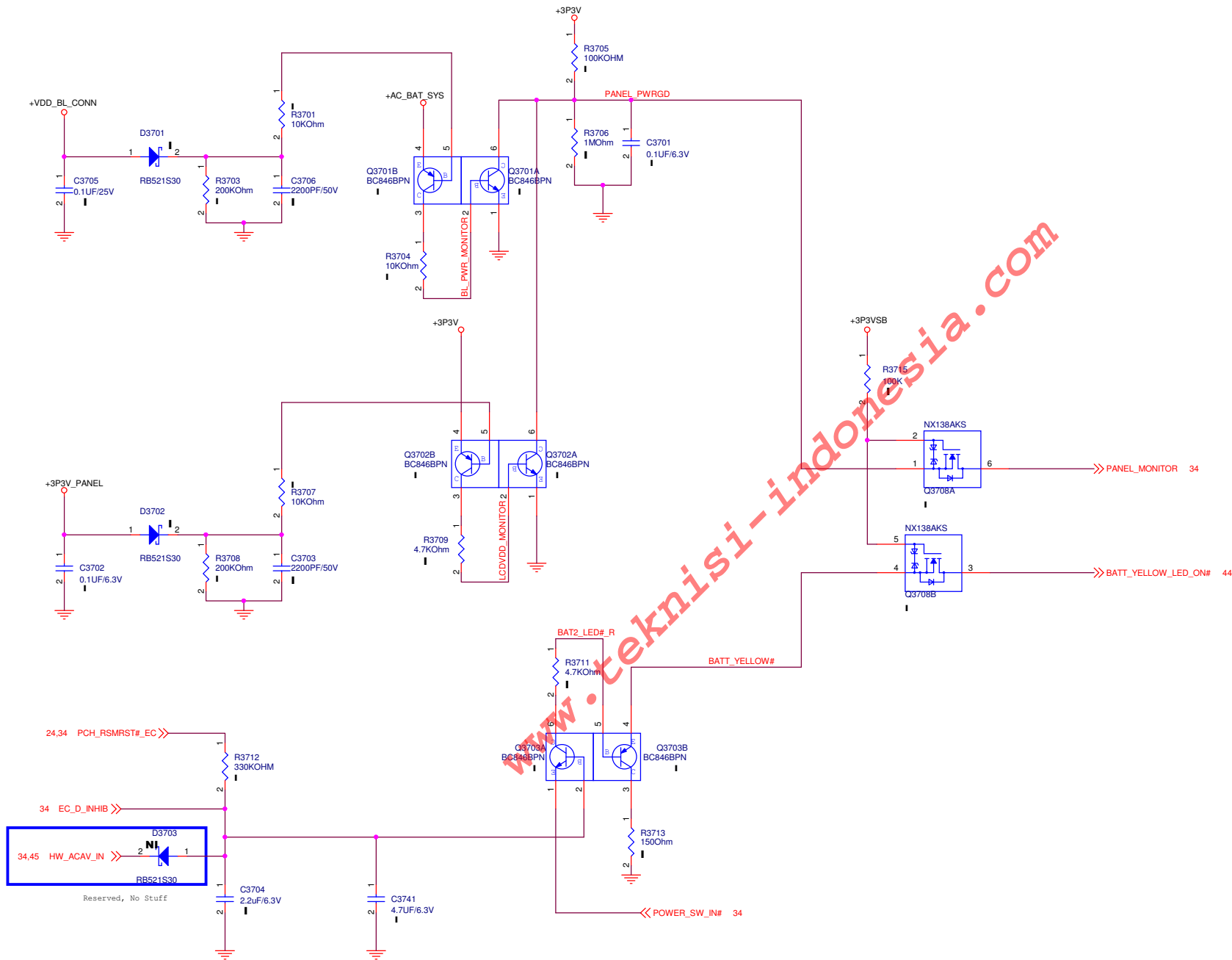
Project Name Nebula

Rev A00

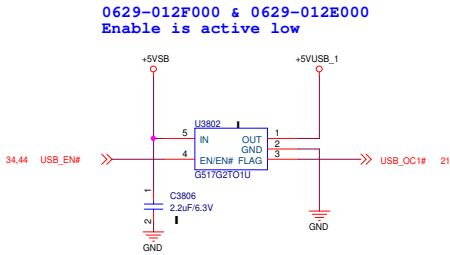
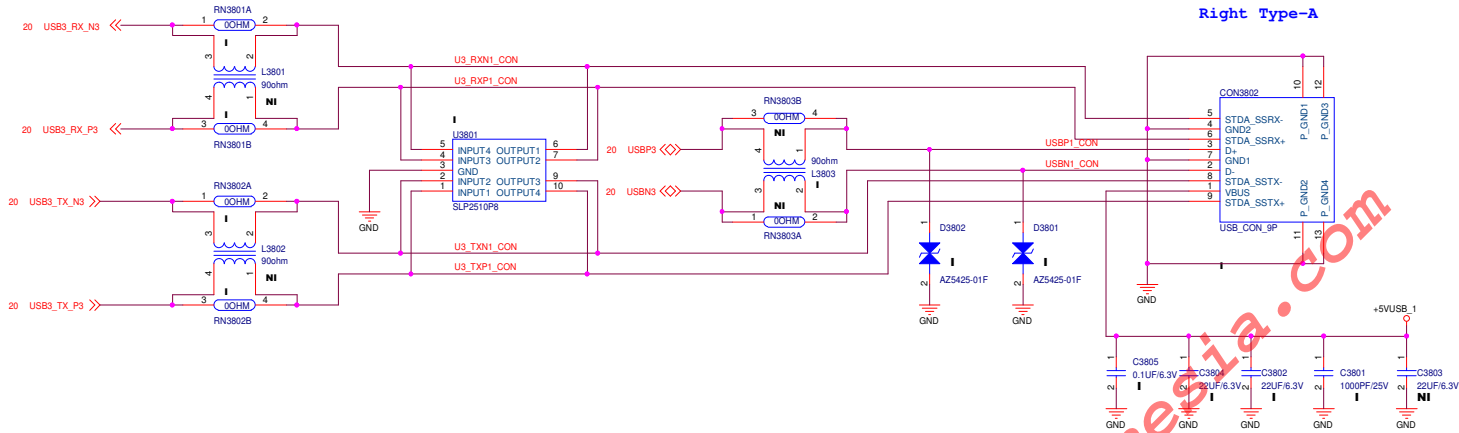
Date: Wednesday, March 27, 2019

Sheet 36 of 96

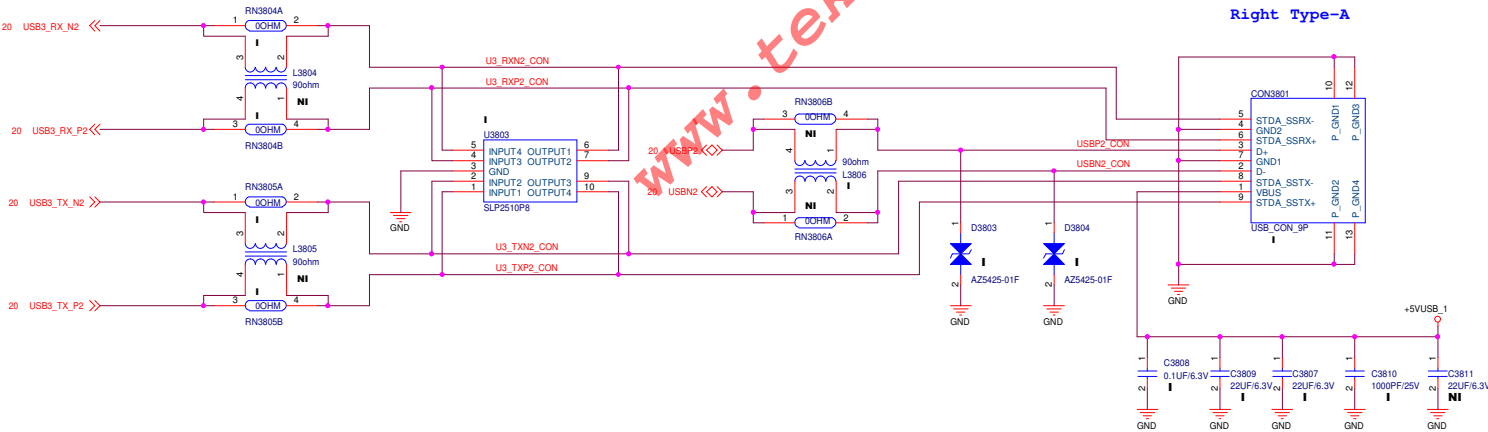
LCD BIST



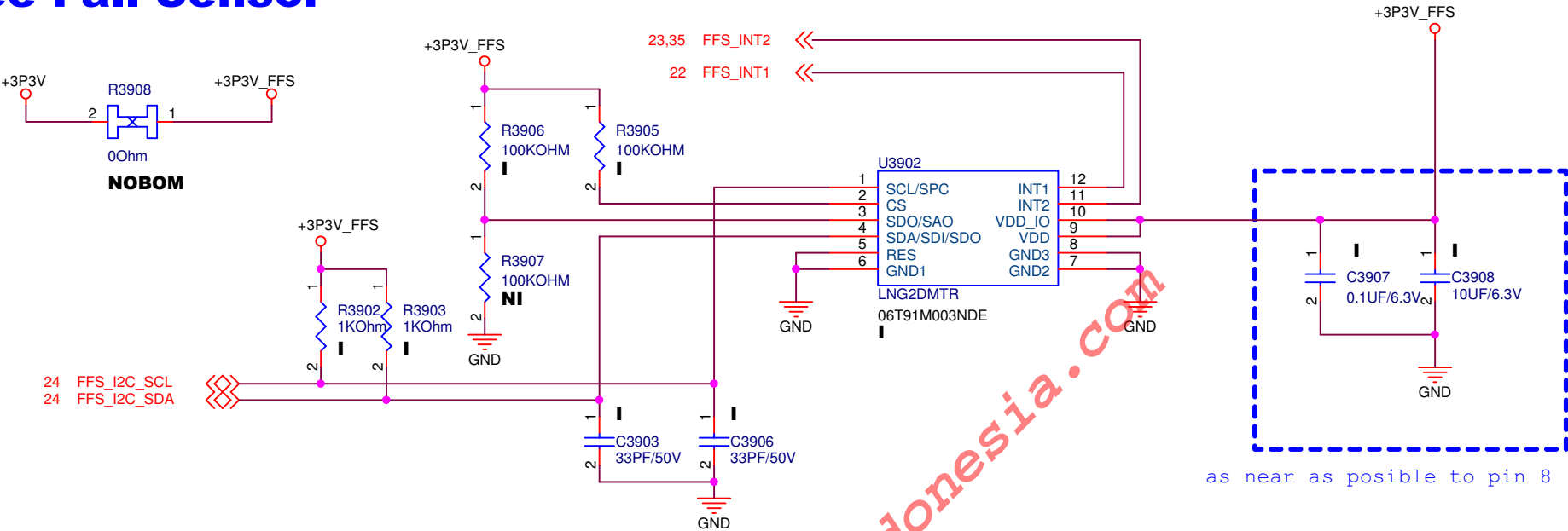
USB3.1 TypeA Port1 & Reapeater (Right side)



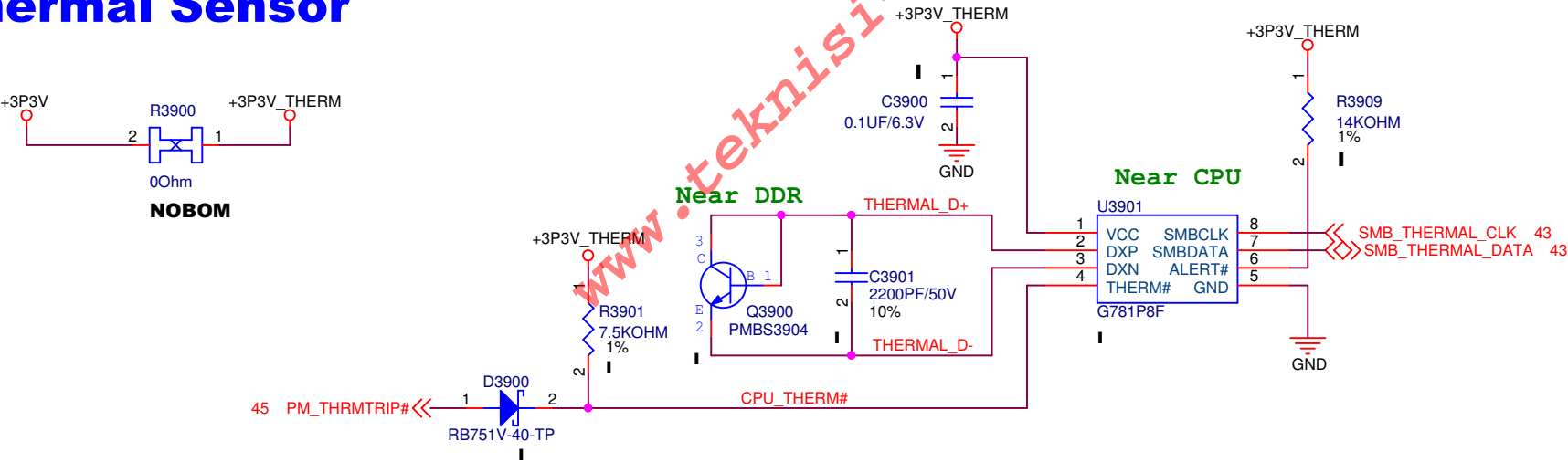
USB3.1 TypeA Port2 & Reapeater (Right side)



Free Fall Sensor



Thermal Sensor



TEMPERATURE (°C)		T_CRIT				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

PEGATRON

Title : **SENSOR**

Pegatron Corp.

Engineer: **EE**

Size

Project Name

Rev

Custom

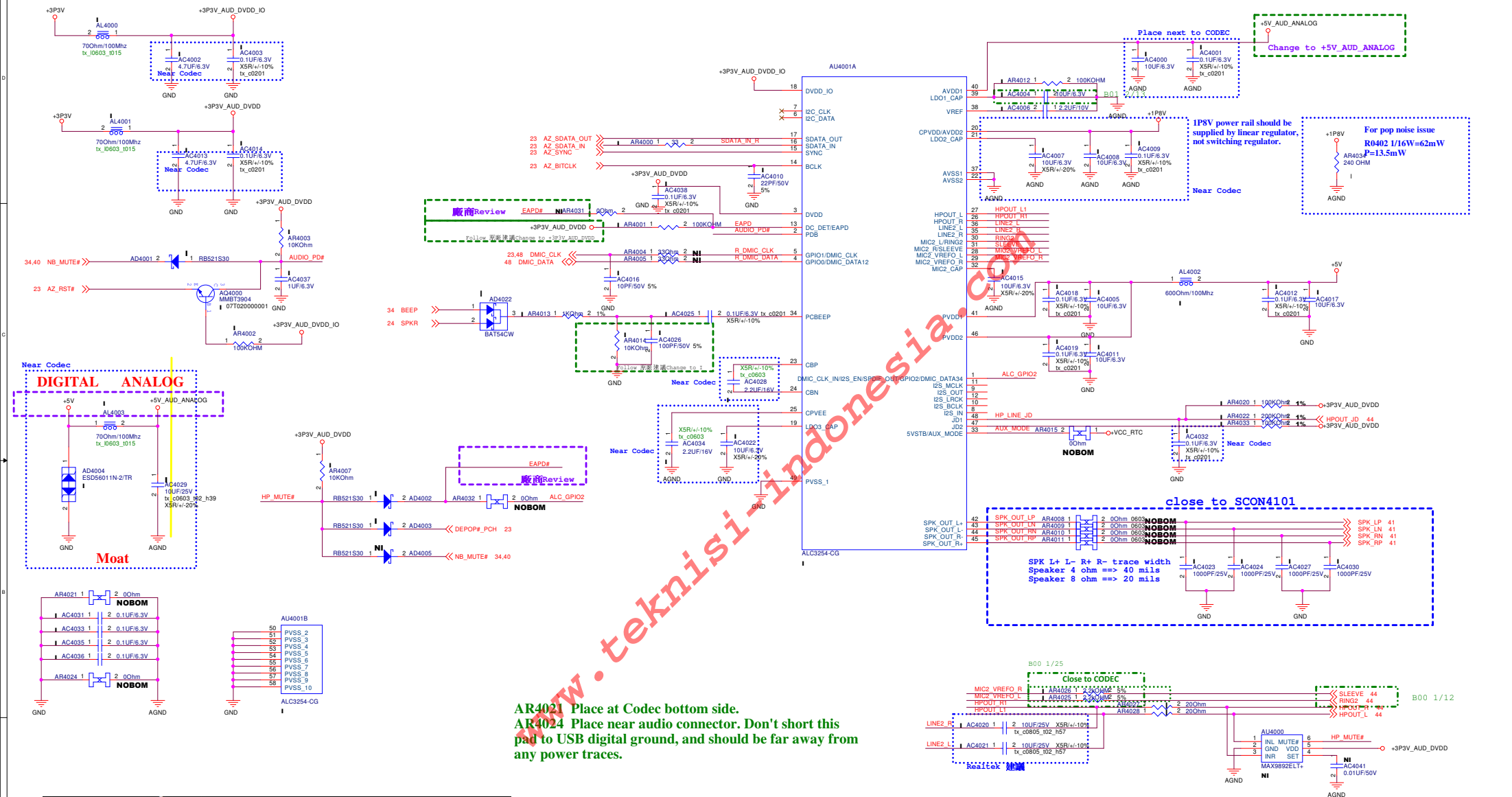
Nebula

A00

Date: **Wednesday, March 27, 2019**

Sheet **39** of **96**

AUDIO CODEC- ALC3254-CG

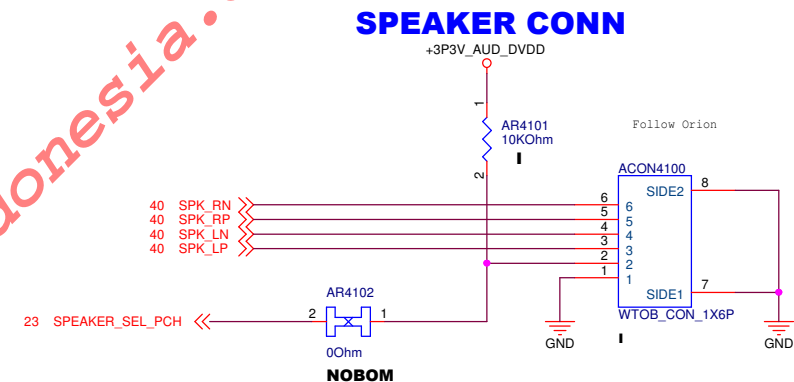
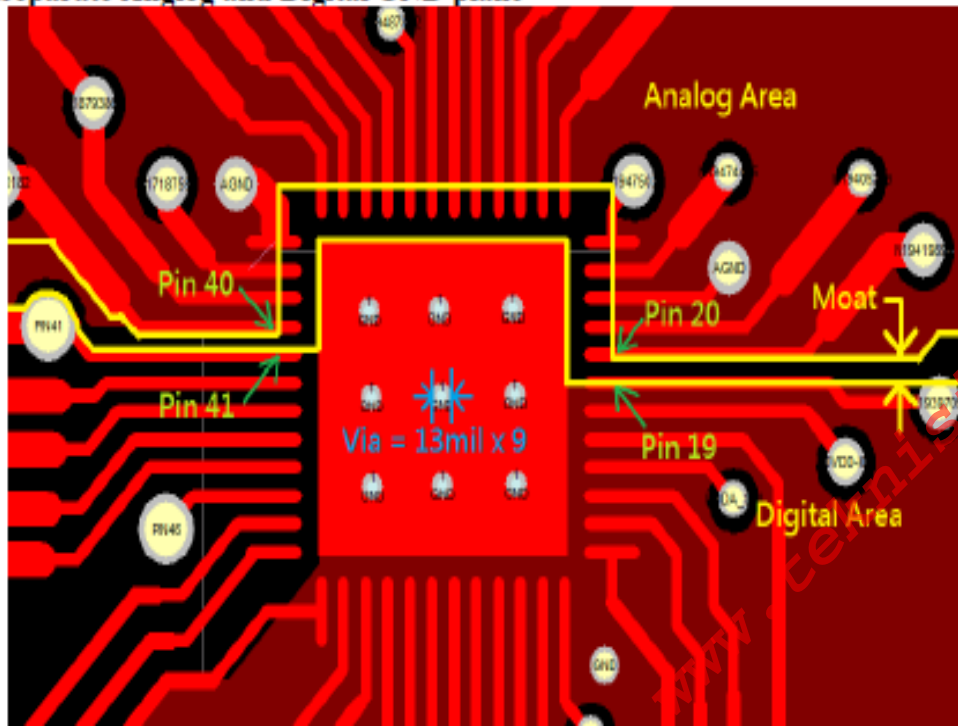


Power Rail	Voltage	Current (max)	Remark
PVDD1	5.0V	1.5A	4ohm speaker
PVDD2	5.0V	1.5A	4ohm speaker
AVDD1	5.0V	20mA	If Line2-in (PORT 1B) not in use
AVDD1	5.0V	120mA	If Line2-in (port 1B) need to support output with headphone amp.
AVDD2	1.8V	20mA	
CPVDD	1.8V	300mA/150mA/80mA	6ohm/16ohm / 32ohm headphone loading
DVDD	3.3V	10mA	
DVDD-I/O	3.3 ~ 1.5V	10mA	

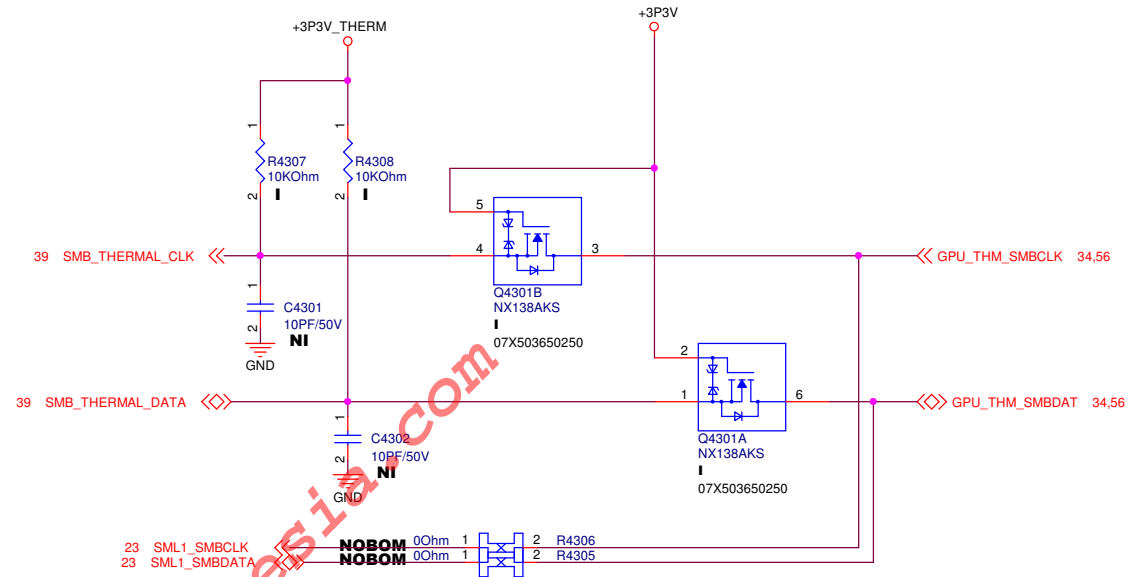
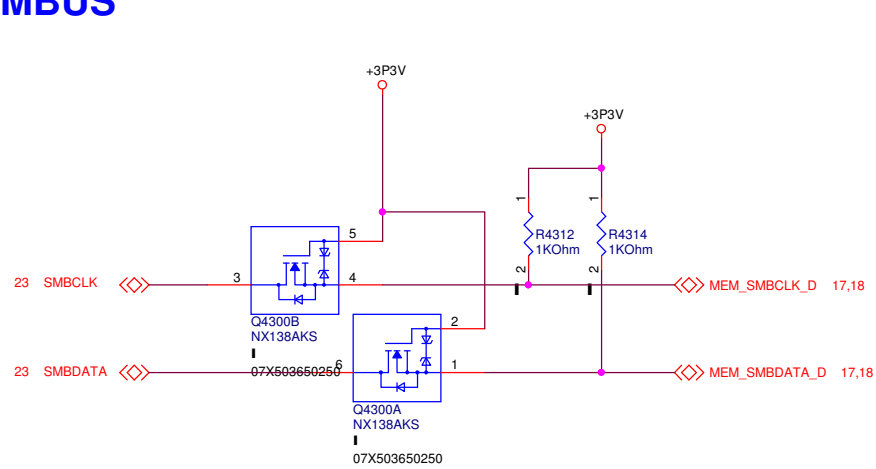
**OMTP/CTIA headset, Headphone, Line-Out,
Microphone input, Line input.**

PCB trace width of Mic1-R/Mic1-L(SLEEVE/RING2) are required at least 40 mil for HP crosstalk consideration, and its length should be as short as possible.

Separate Analog and Digital GND plane

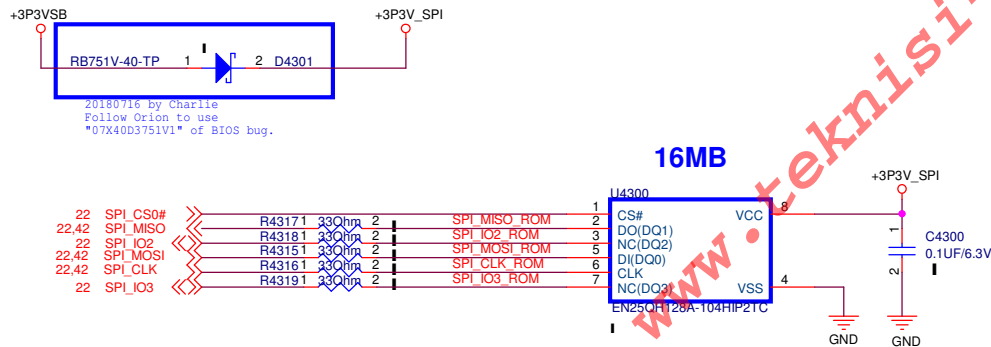


SMBUS

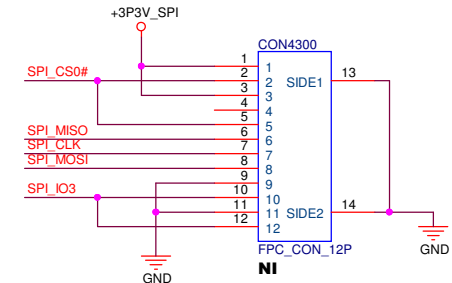


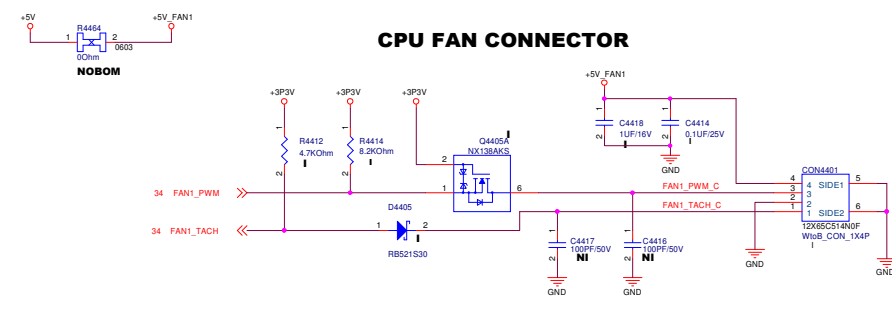
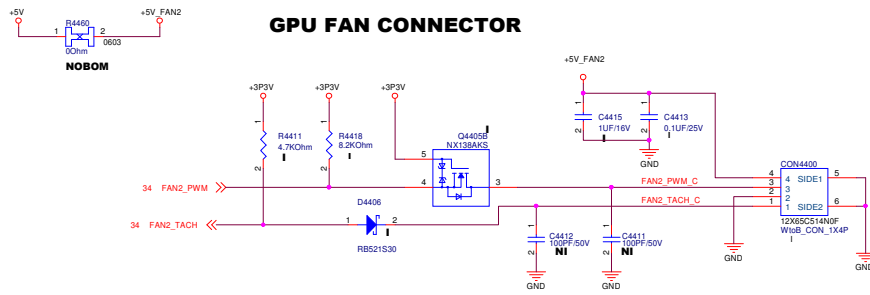
PCH side pull high +3P3VSB 1K

SPI ROM (Quad I/O Supported)

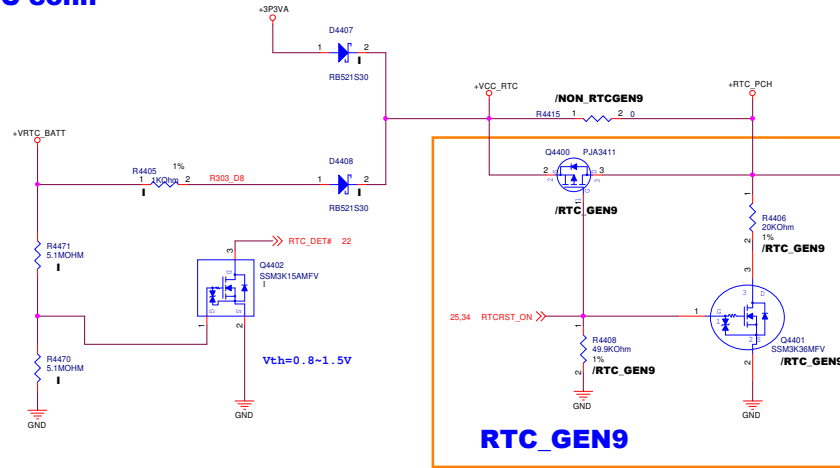


For ROM Flashing

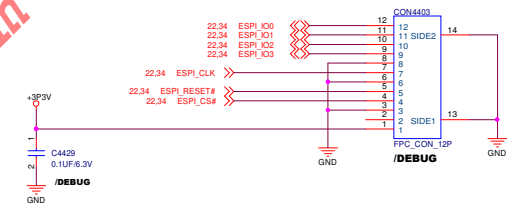




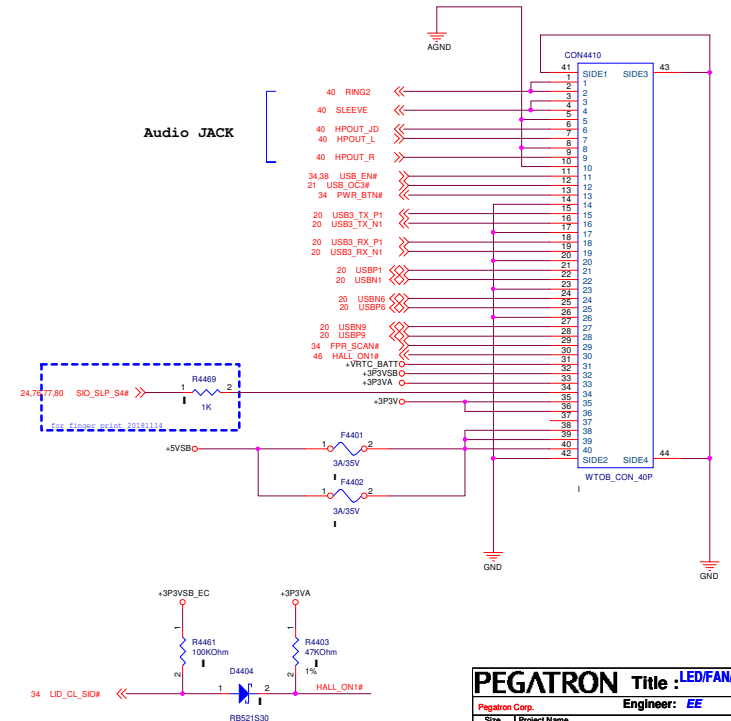
RTC conn



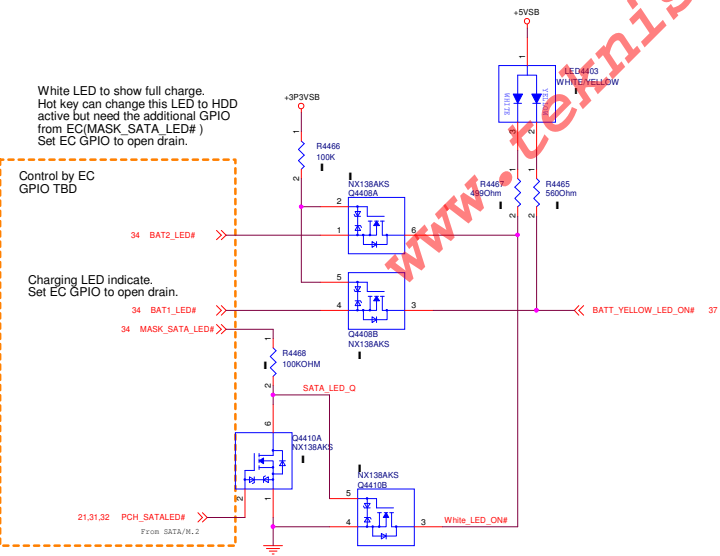
eSPI DEBUG PORT



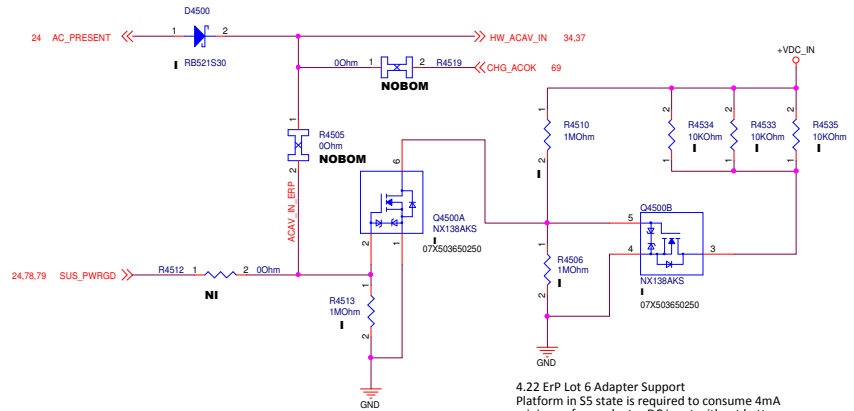
IO Connector



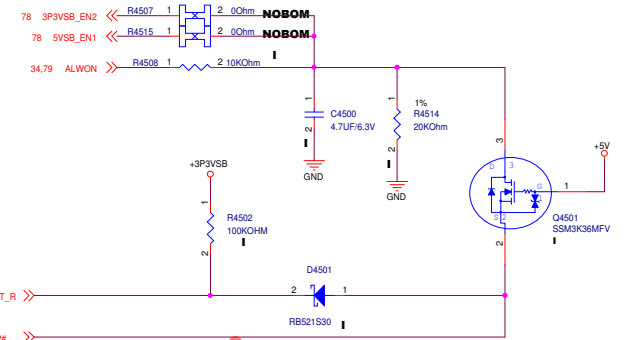
LED



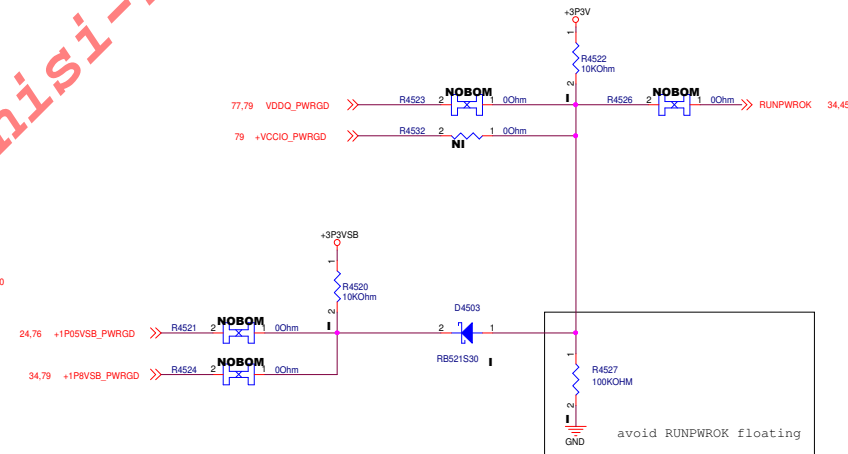
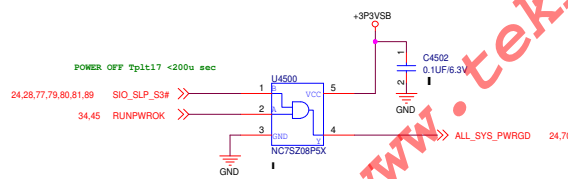
ACAV_IN Circuit



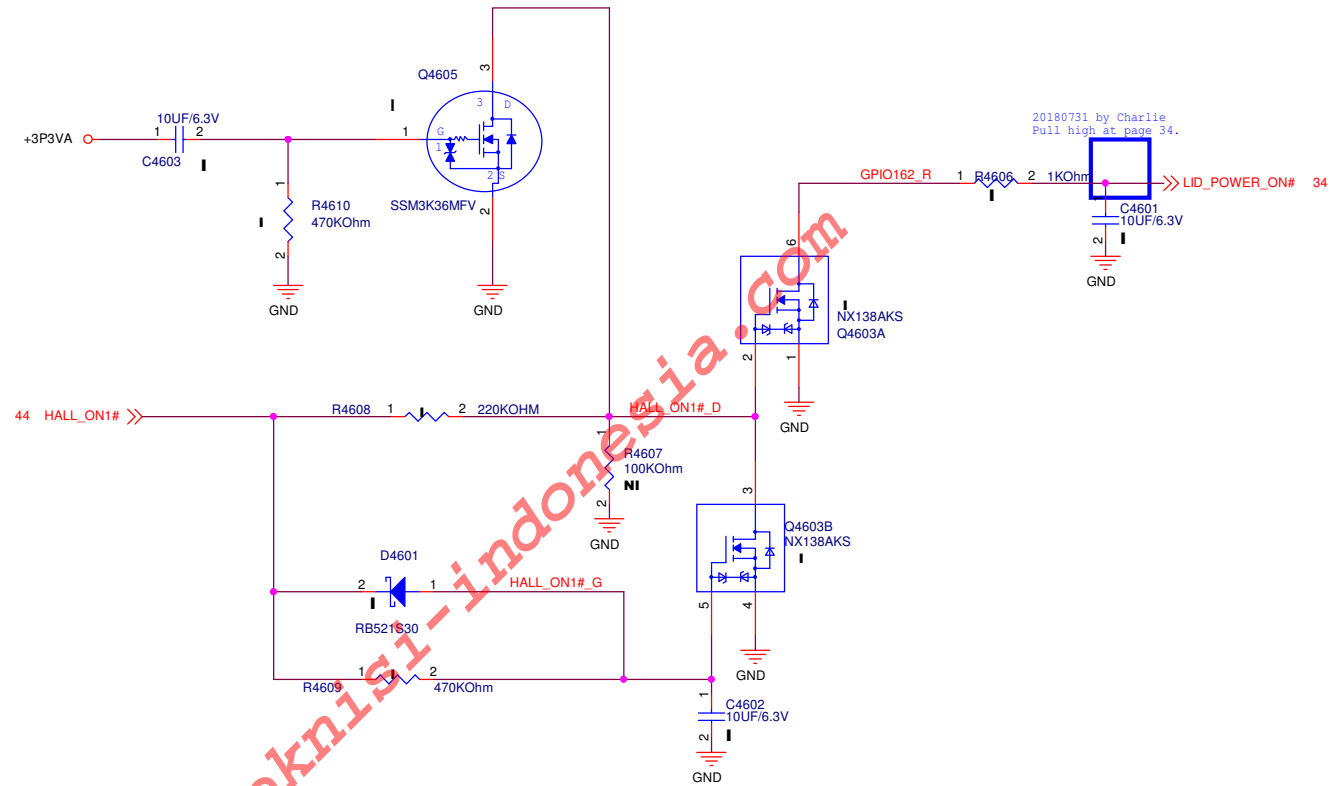
Thermal CMP Circuit



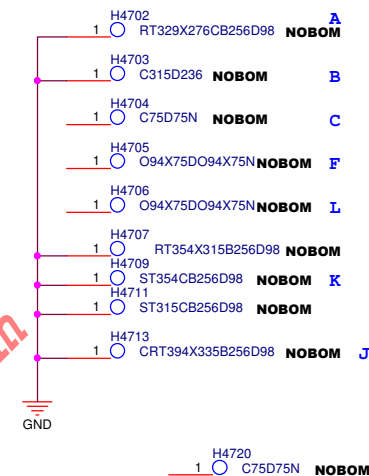
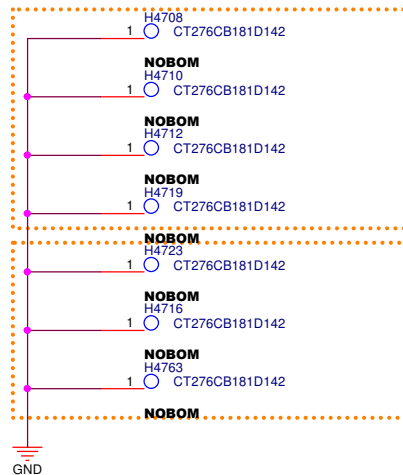
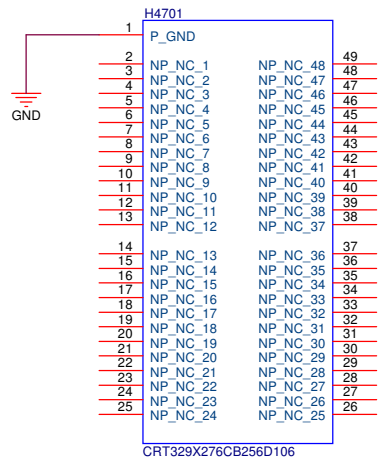
POWER GOOD DETECTOR



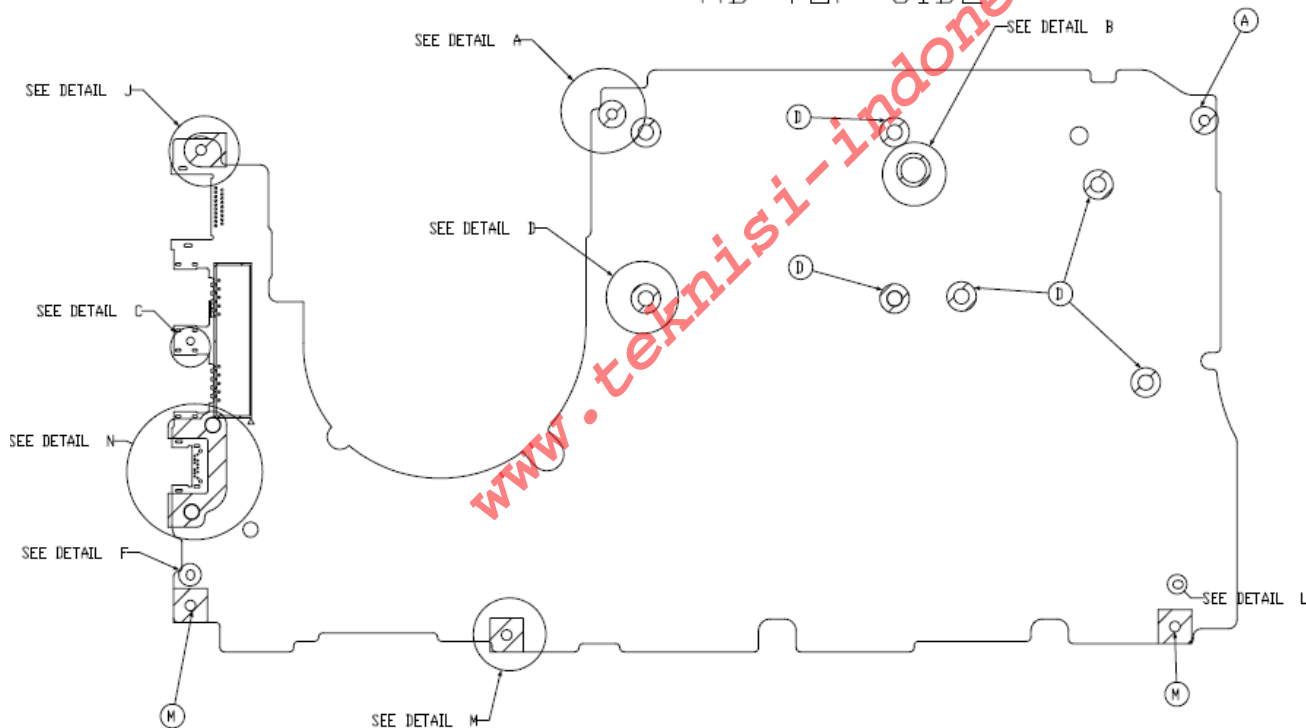
LID OPEN POWER ON



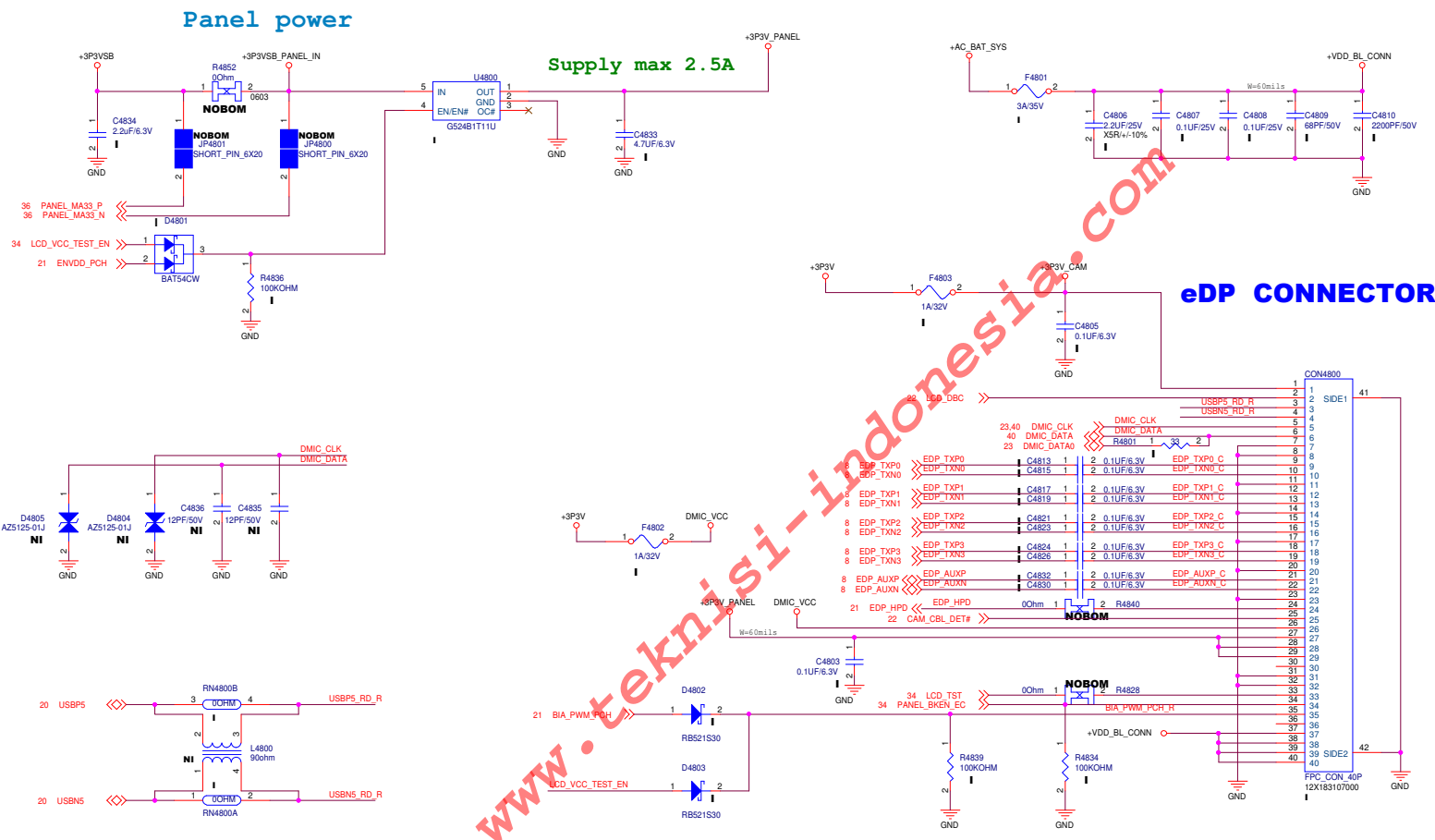
H4701 Thermal 要求修改 2018.10.25



MB TOP SIDE



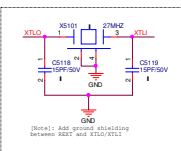
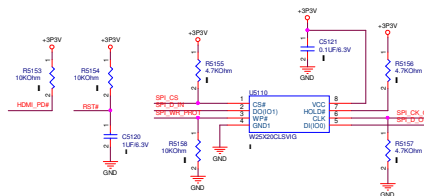
PEGATRON		Title: Label_Screw	
Pegatron Corp.		Engineer: EE	
Size B	Project Name Nebula	Rev A00	
Date: Wednesday, March 27, 2019		Sheet 47 of 96	



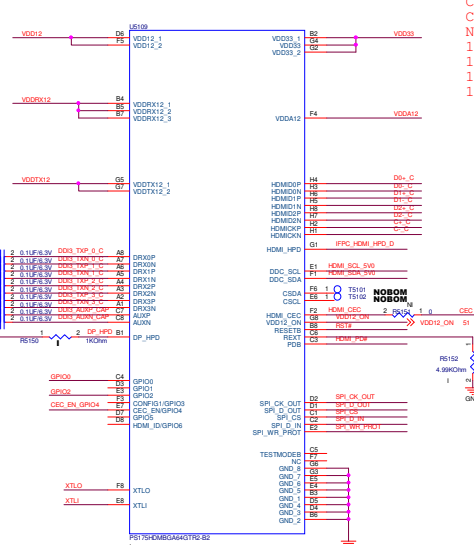
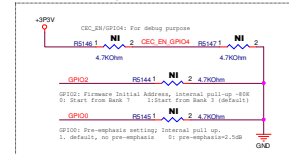
Reserve Page

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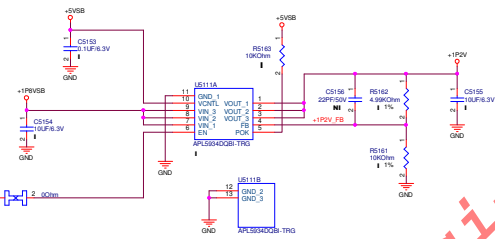
PEGATRON		Title : XXX	
Pegatron Corp.		Engineer: EE	
Size B	Project Name Nebula		Rev A00
Date: Wednesday, March 27, 2019		Sheet	50 of 96



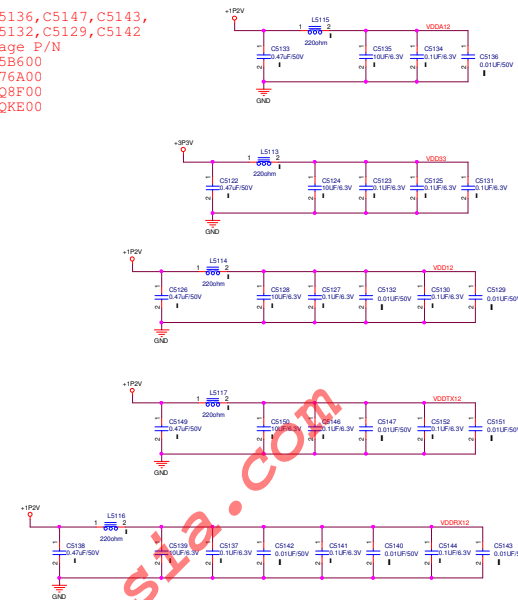
Power On Configuration



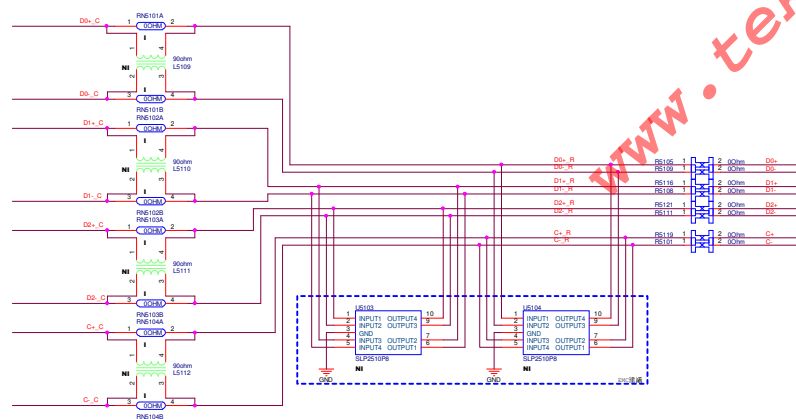
X01 add LDO +1P2V output



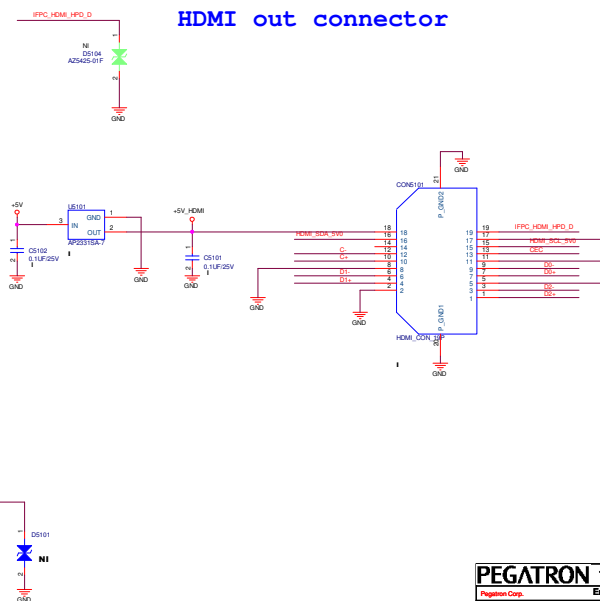
C5140,C5136,C5147,C5143.
C5151,C5132,C5129,C5142
Need chage P/N
1A10-005B600
1A10-0176A00
1A10-00Q8F00
1A10-00QKE00

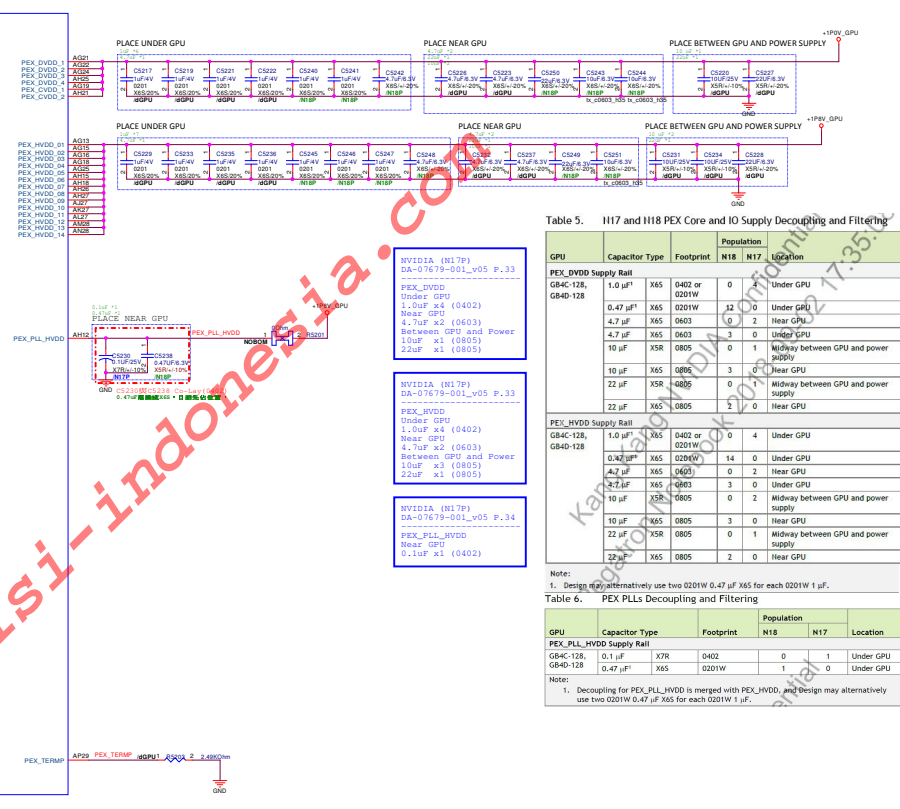


HDMI



HDMI out connector





GPU	Capacitor Type	Footprint	Population		Location
			N18	N17	
PEC_HVDD Supply Rail GBAC-118, GBAD-128	1.0 μ F	X65 0402 or 0201W	0	4	Under GPU
	0.47 μ F	X65 0201W	32	0	Under GPU
	4.7 μ F	X65 0603	0	2	Heater Chip
	4.7 μ F	X65 0603	0	0	Under GPU
	10 μ F	X58 0805	0	1	Midway between GPU and power supply
	22 μ F	X65 0806	3	0	Heater GPU
	10 μ F	X58 0805	0	1	Midway between GPU and power supply
	22 μ F	X65 0805	5	0	Heater GPU
PEC_HVDD Supply Rail GBAC-118, GBAD-128	1.0 μ F	X65 0402 or 0201W	0	4	Under GPU
	0.47 μ F	X65 0201W	14	0	Under GPU
	4.7 μ F	X65 0603	0	2	Heater GPU
	4.7 μ F	X65 0603	3	0	Under GPU
	10 μ F	X58 0805	0	2	Midway between GPU and power supply
	10 μ F	X65 0805	3	0	Heater GPU
	22 μ F	X58 0805	0	1	Midway between GPU and power supply
	22 μ F	X65 0805	2	0	Heater GPU

Note:

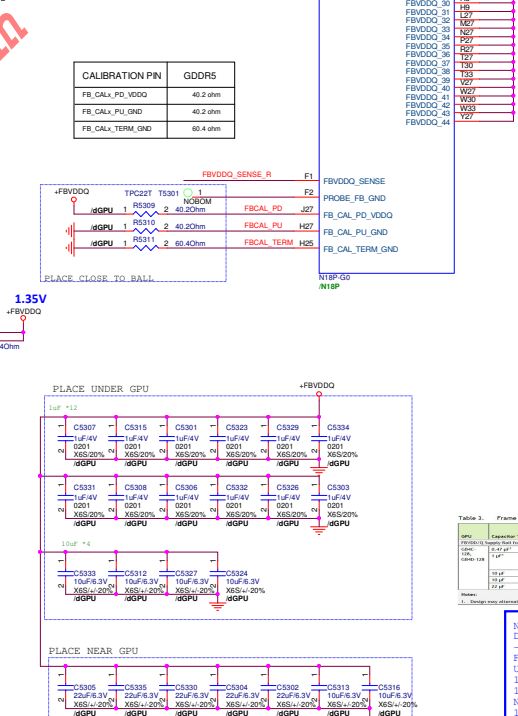
1. Design may alternatively use two 0201W 0.47 μ F X65 for each 0201W 1 μ F.

Table 6. PEX PLLs Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population		Location	
			N18	N17		
PEX_PLL_HVDD Supply Rail						
GB4C-128,	0.1 μ F	X7R	0402	0	1	Under GPU
GB4D-128	0.47 μ F ¹	X6S	0201W	1	0	Under GPU

Note:

- Decoupling for PEX_PLL_HVDD is merged with PEX_HVDD, and Design may alternatively use two 0201W 0.47 μ F X65 for each 0201W 1 μ F.



PEGATRON		Title: GPU_FRAME_BUFFER	
Pegatron Corp.		Engineer: WJ	
Size	Project Name	Nebula	Rev A00
Custom			
Date: Wednesday, March 27, 2019		Sheet 53	of 96

XS_PLLVDD
Under GPU (Put at GPCPLL_AVDD side)
No capacitors

SP_PLLVDD/VID_PLVDD
Under GPU
0.1uF x2 (0402)

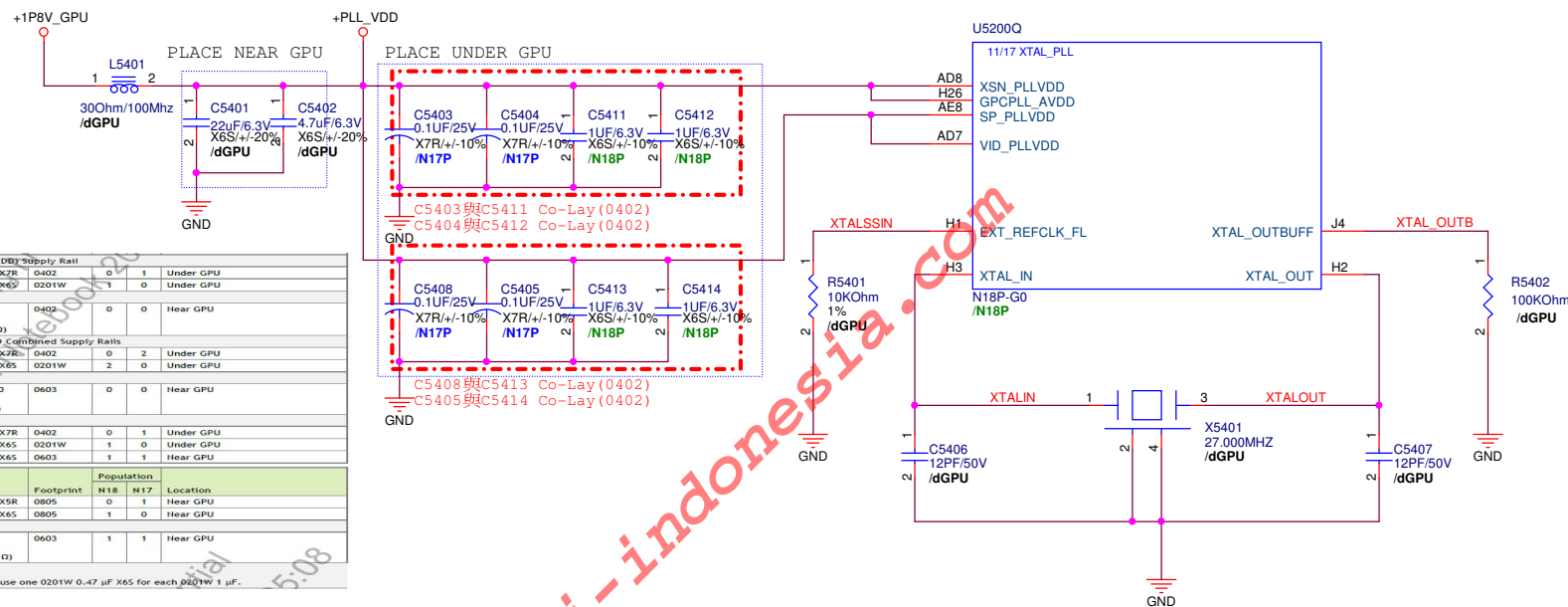
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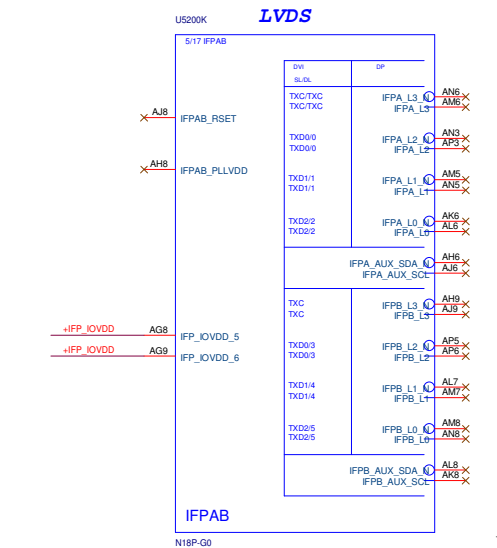
GPCPLL_AVDD
Under GPU
0.1uF    x1  (0402)
Near GPU
4.7uF    x1  (0603)
22 uF    x1  (0805)

```

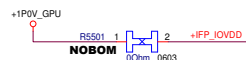
Note:

1. Design may alternatively use one 0201W 0.47 μ F X6S for each 0201W 1 μ F.





NVIDIA N17P
DA-07679-001_v05 P.37
IFPCD_PLLVDD
Under GPU
0.1uF x2 (0402)



C5514與C5502 Co-Lay (0402)
C5515與C5503 Co-Lay (0402)
C5516與C5504 Co-Lay (0402)
C5517與C5505 Co-Lay (0402)
C5518與C5506 Co-Lay (0402)
C5519與C5507 Co-Lay (0402)

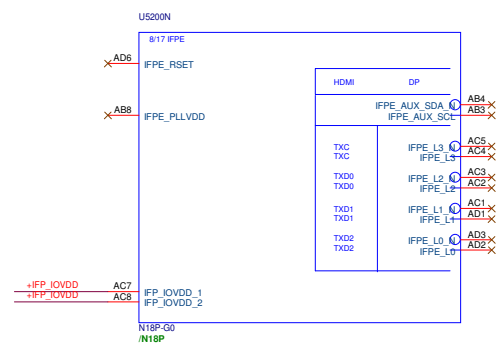
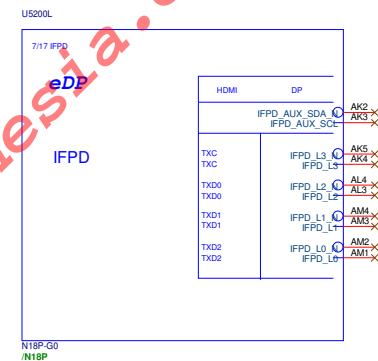
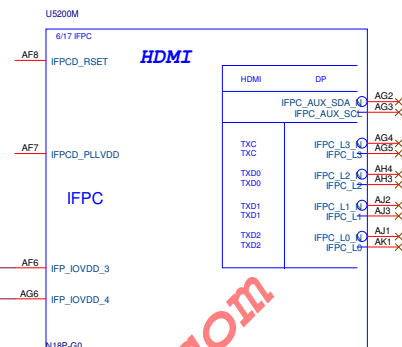
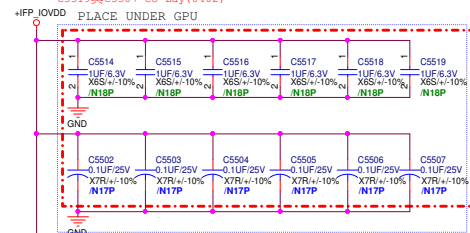


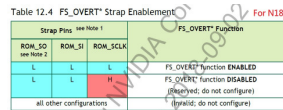
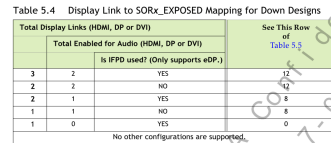
Table 7. IFPy_IOVDD Decoupling and Filtering

GPU	Type	Footprint	Population	N18	N17	Location
IFPy_IOVDD Supply Rail						
GB4C-128	0.47 uF	X7R	0402	0	6	Under GPU; 1 per ball
GB4D-128	0.47 uF	X6S	0201W	6	6	Under GPU; 1 per ball
	1.0 uF	X6S	0402 or 0201W	6	3	Near GPU
	0.47 uF	X6S	0201W	6	0	Near GPU
	4.7 uF	X6S	0603	3	3	Near GPU
Bead Type						
	180 Ohm @ 100 MHz		0603	0	0	Near GPU

Note:
1. Design may alternatively use one 0201W 0.47 uF X6S for each 0201W 1 uF.
2. Design may alternatively use two 0201W 0.47 uF X6S for each 0201W 1 uF.

NVIDIA (N17P)
DA-07679-001_v05 P.36

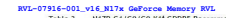
IFPy_IOVDD
Under GPU
0.1uF x5 (0402)
Near GPU
4.7uF x3 (0603)
1uF x3 (0402)



Row Index	Strap Pins			Resulting SOR _X EXPOSED Enablements			
	ROM_S0	ROM_SI	ROM_SCLK	SOR ₁ _EXPOSED	SOR ₂ _EXPOSED	SOR ₃ _EXPOSED	SOR ₀ _EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	H	ENABLED	ENABLED	ENABLED	disabled
13	L	H	L	ENABLED	ENABLED	disabled	ENABLED
12	L	H	H	ENABLED	ENABLED	disabled	disabled
8	H	H	H	ENABLED	disabled	disabled	disabled
0	H	H	M	disabled	disabled	disabled	disabled
	M	X	X	(Reserved; do not configure)			
All other Strap Configurations				(Reserved)			

Note 1: Configurations other than the two listed in Table 12.4 must be avoided, as otherwise damage to *stap* inputs may result.

Note 2: The ROM *SO* pin should be pulled low using a 10 k Ω resistor instead of a resistor.



Allowed						
---------	--	--	--	--	--	--

Memory Security	Memory Configuration	Firmware	Vendor	Manufacturer Part Number	Die ID	Die Revision	Memory Size	Code Address	Full Path	Status
8 GB	256MBx2	1.30V and 1.5V	SamSung	K4G41SFE2H-EC23	B-die	D0d	7 Gbps	N/A	Full	Production ready
			SamSung	K4G41SFE2H-EC23	B-die	D0d	8 Gbps	N/A	N/A	Substitution allowed with vendor
			Micros	MT171J256M2HDF-70A	A-die	D0d	8 Gbps	N/A	Full	Production ready
			Micros	MT171J256M2HDF-70A	A-die	D0d	8 Gbps	N/A	Full	Production ready with vendor
			Hynix	H5GQ8B4M4EABR-EC	A-die	DQd	7 Gbps	N/A	Full	Full production ready
			Hynix	H5GQ8B4M4EABR-EC	A-die	DQd	8 Gbps	N/A	N/A	Substitution allowed with vendor
			Micros	MT171J256M2HDF-70B	B-die	D0a	7 Gbps	N/A	Full	Full production ready
			Micros	MT171J256M2HDF-70B	B-die	D0a	8 Gbps	N/A	N/A	Substitution allowed with vendor
			Hynix	H5GQ8B4M4EABR-EC	B-die	DQd	7 Gbps	N/A	Full	Full production ready
			Hynix	H5GQ8B4M4EABR-EC	B-die	DQd	8 Gbps	N/A	N/A	Substitution allowed with vendor

Table 4. N18P-G0 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBDVD/Q	Vendor	Manufacturer Part Number	The Revision	Storage	Memory Speed Grade	Date Code/Alert	Qual Plan	Status
8 Gb	256Mx32		Micro [®]	MT51255Mx32DF-80-B	B-die	Q1	8 Gbps	N/A	Full	Production candidate
			Hyntix	H5G6B32-44LR-R2C	A-die	Q1	8 Gbps	N/A	Full	Production candidate
			TBD	Samsung [®]	KAG0825FC-HC25	C-die	Q1	8 Gbps	N/A	Full

RVL-08928-001_v05_N18x GeForce Memory RVL



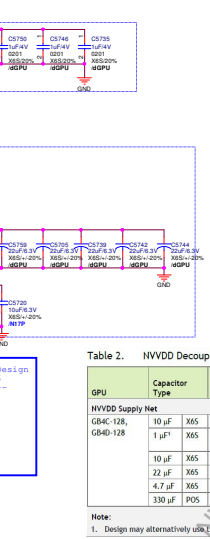
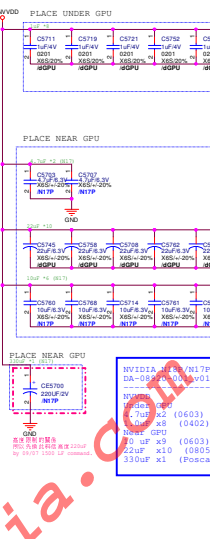
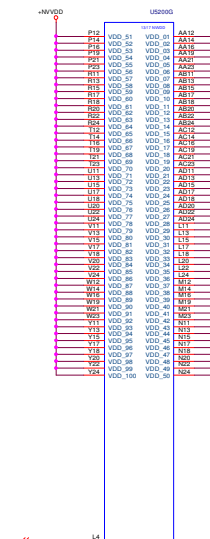
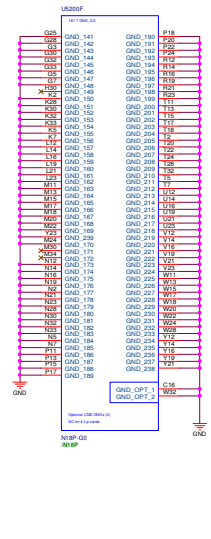
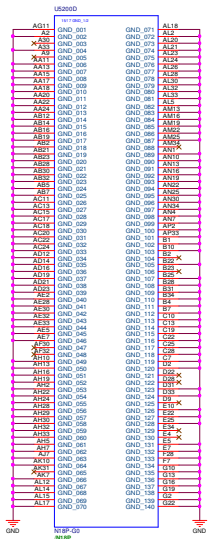
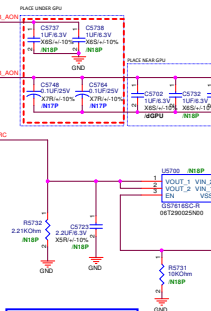


Table 2. NVDD Decoupling and Filtering

GPU	Capacitor Type	Footprint	Population	N18	N17	Location
NVDD Supply Net						
GB4C-128, GB4D-128	10 μ F	X65	0603	34	21	Under GPU
	1 μ F	X65	0402 or 0201W	33	13	Under GPU
	10 μ F	X65	0603	0	11	Near GPU
	22 μ F	X65	0805	15	10	Near GPU
	4.7 μ F	X65	0603	0	2	Near GPU
	330 μ F	POS	7343	0	1	Near GPU

Note:
1. Design may alternatively use 0201W 0.47 μ F X65 for each 0201W 1 μ F.

C5737, C5748 Co-Lay (0402)
C5738, C5744 Co-Lay (0402)

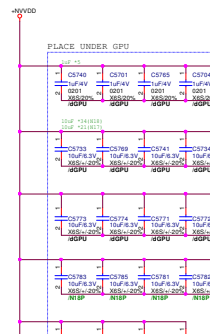


NVIDIA (N17P)
DA-07679-001_v05 P.40
1V8_AON
Under GPU
0.1 μ F x2 (0402)
Near GPU
1.0 μ F x1 (0402)
4.7 μ F x1 (0603)

Table 9. VDD_AON and VDD_Main Decoupling

GPU	Capacitor Type	Footprint	Population	N18	N17	Location
N17 VDD18 (N18 NC) Supply Rail						
GB4C-128, GB4D-128	0.1 μ F	X78	0402	N/A	2	Under GPU
	1.0 μ F	X65	0603	N/A	1	Near GPU
	4.7 μ F	X65	0603	N/A	1	Near GPU
1V8_AON Supply Rail						
GB4C-128, GB4D-128	0.1 μ F	X78	0402	0	2	Under GPU
	0.47 μ F	X65	0201W	4	0	Under GPU
	1.0 μ F	X65	0402 or 0201W	0	1	Near GPU
	0.47 μ F	X65	0201W	6	0	Near GPU
	4.7 μ F	X65	0603	3	1	Near GPU

Note:
1. Design may alternatively use two 0201W 0.47 μ F X65 for each 0201W 1 μ F.



NVIDIA (N17P)
DA-07679-001_v05 P.40
VDD18
Under GPU
0.1 μ F x2 (0402)
Near GPU
1.0 μ F x1 (0402)
4.7 μ F x1 (0603)

Table 9. VDD_AON and VDD_Main Decoupling

GPU	Capacitor Type	Footprint	Population	N18	N17	Location
N17 VDD18 (N18 NC) Supply Rail						
GB4C-128, GB4D-128	0.1 μ F	X78	0402	N/A	2	Under GPU
	1.0 μ F	X65	0603	N/A	1	Near GPU
	4.7 μ F	X65	0603	N/A	1	Near GPU
1V8_AON Supply Rail						
GB4C-128, GB4D-128	0.1 μ F	X78	0402	0	2	Under GPU
	0.47 μ F	X65	0201W	4	0	Under GPU
	1.0 μ F	X65	0402 or 0201W	0	1	Near GPU
	0.47 μ F	X65	0201W	6	0	Near GPU
	4.7 μ F	X65	0603	3	1	Near GPU

Note:
1. Design may alternatively use two 0201W 0.47 μ F X65 for each 0201W 1 μ F.



NVIDIA (N18P/N17P Co-Design)
DA-07679-001_v01 P.16
NVDD18
Under GPU
10 μ F x2 (0603)
4.7 μ F x1 (0402)
1.0 μ F x5 (0402)

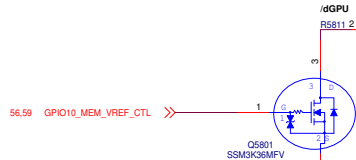
Table 9. VDD_AON and VDD_Main Decoupling

GPU	Capacitor Type	Footprint	Population	N18	N17	Location
NVDD18 Supply Rail						
GB4C-128, GB4D-128	10 μ F	X65	0603	34	21	Under GPU
	1 μ F	X65	0402 or 0201W	33	13	Under GPU
	10 μ F	X65	0603	0	11	Near GPU
	22 μ F	X65	0805	15	10	Near GPU
	4.7 μ F	X65	0603	0	2	Near GPU
	330 μ F	POS	7343	0	1	Near GPU

Note:
1. Design may alternatively use 0201W 0.47 μ F X65 for each 0201W 1 μ F.

GDDR5 Mode H Mapping

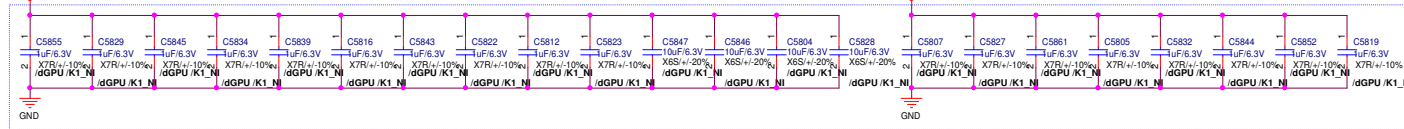
GB2B-64	Ch0 0..31	GB4B-128	Ch1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3 BA3	CMD17	A3 BA3
CMD2	A2 BA0	CMD18	A2 BA0
CMD3	A4 BA2	CMD19	A4 BA2
CMD4	A5 BA1	CMD20	A5 BA1
CMD5	WE*	CMD21	WE*
CMD6	A7 A8	CMD22	A7 A8
CMD7	A6 A11	CMD23	A6 A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12 RFU	CMD25	A12 RFU
CMD10	A0 A10	CMD26	A0 A10
CMD11	A1 A9	CMD27	A1 A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*



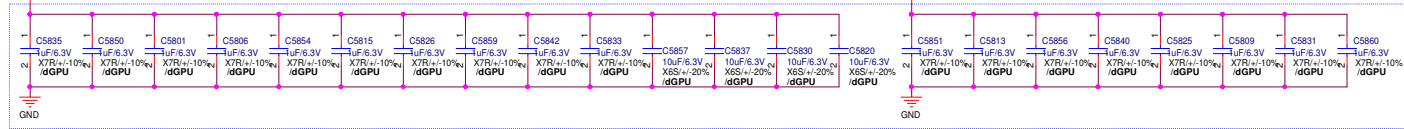
NVIDIA (N17P)
DG-07875-001_v08 page.160

+FBVDDQ at DRAM Side
Under GPU
1uF x10 (0402)
10uF x4 (0603)
1uF x8 (0402)
Near GPU
10uF x2 (0603)

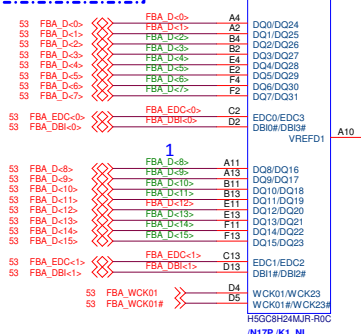
Place Under DRAM M3



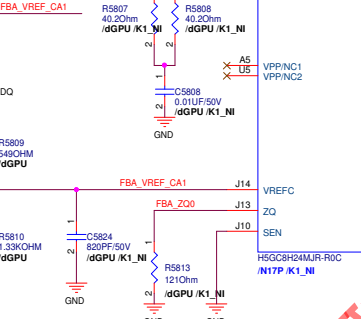
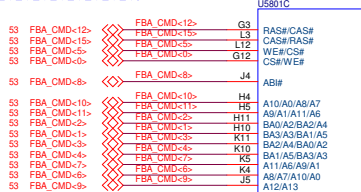
Place Under DRAM M4



DRAM M3

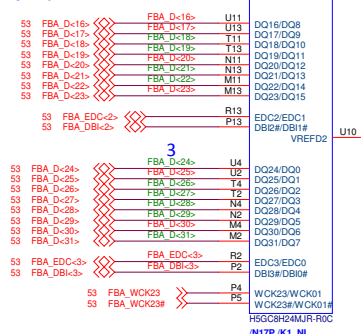


DRAM M3

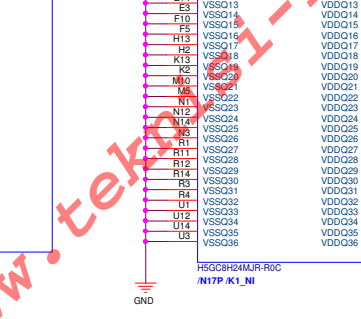
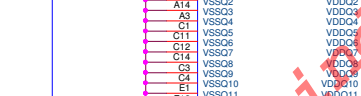
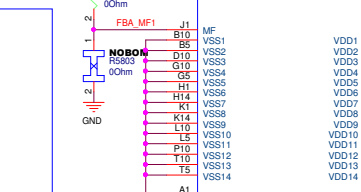


Note : At least 2 GND vias and 2 power vias for each decoupling capacitor

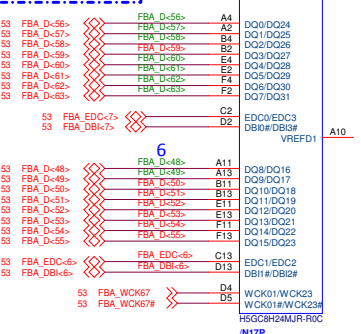
DRAM M4



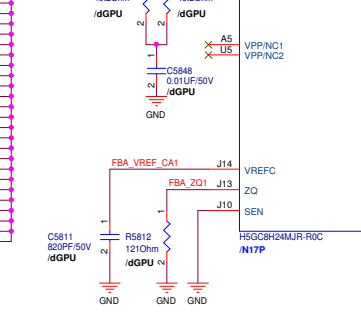
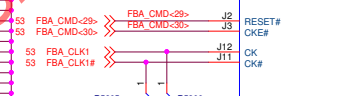
DRAM M4



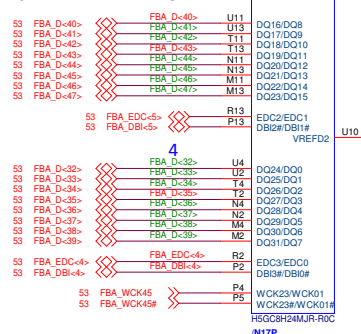
DRAM M4



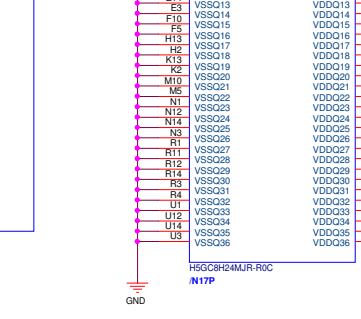
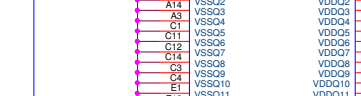
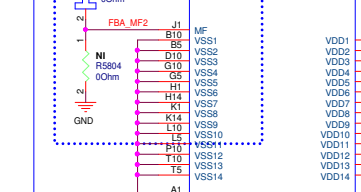
DRAM M4



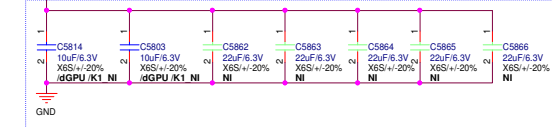
DRAM M4



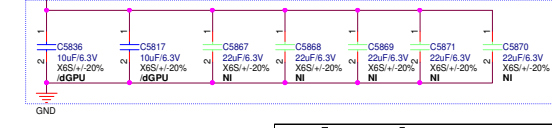
DRAM M4



Place Near DRAM M3



Place Near DRAM M4

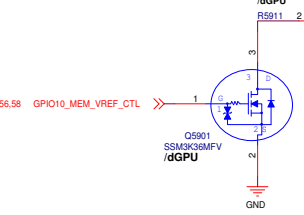


DRAM M1

MEMORY : FBB Partition 31:0 (Normal)
MEMORY : FBB Partition 63:32 (Mirror)

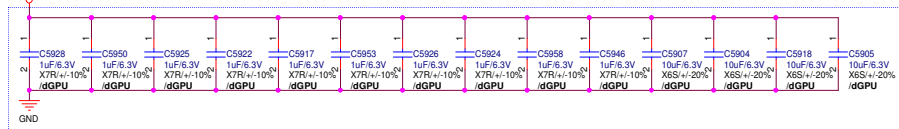
GDDR5 Mode H Mapping

GB2B-64	Ch0 0.31	GB2B-64	Ch1 32.63
GB4B-128		GB4B-128	
GB4C-128		GB4C-128	
CMD0	CS*	CMD16	CS*
CMD1	A3 BA3	CMD17	A3 BA3
CMD2	A2 BA0	CMD18	A2 BA0
CMD3	A4 BA2	CMD19	A4 BA2
CMD4	A5 BA1	CMD20	A5 BA1
CMD5	WE*	CMD21	WE*
CMD6	A7 A8	CMD22	A7 A8
CMD7	A6 A11	CMD23	A6 A11
CMD8	ABI*	CMD24	ABI*
CMD9	A12 RFU	CMD25	A12 RFU
CMD10	A0 A10	CMD26	A0 A10
CMD11	A1 A9	CMD27	A1 A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*

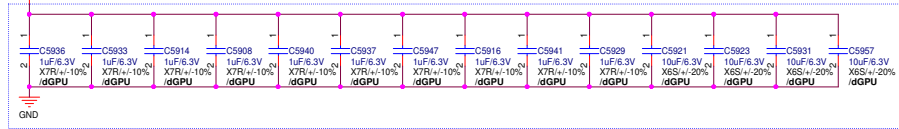


NVIDIA (N17P)
DG-07875-001_v08 page.160
+FBVDDQ at DRAM Side
Under GPU
1uF x10 (0402)
10uF x4 (0603)
1uF x8 (0402)
Near GPU
10uF x2 (0603)

Place Under DRAM M1

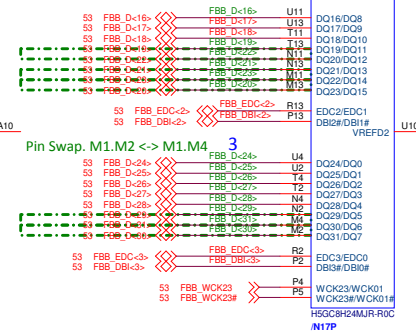


Place Under DRAM M2

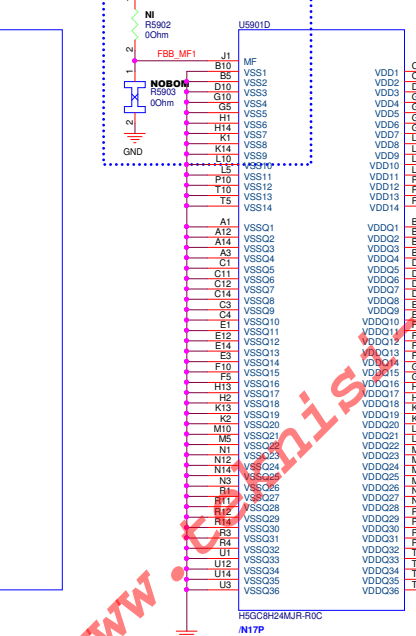


Pin Swap. M1.M11 <=> M1.M13
Pin Swap. M1.M13 <=> M1.M11
Pin Swap. M1.M11 <=> M1.M11

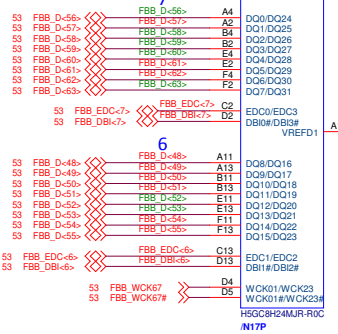
Normal



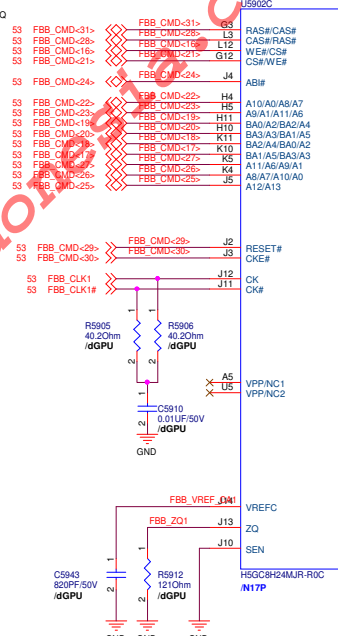
DRAM M1



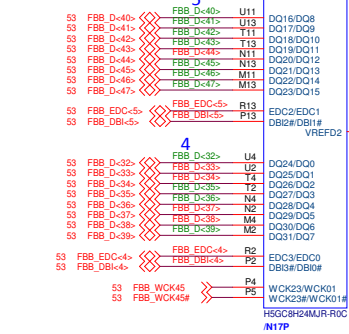
DRAM M2



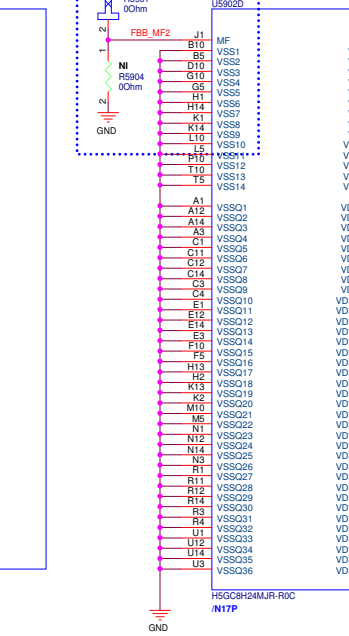
DRAM M2



Mirror

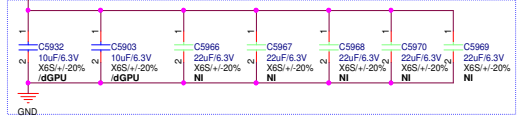


DRAM M2

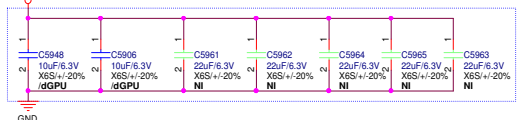


Note : At least 2 GND vias and 2 power vias for each decoupling capacitor

Place Near DRAM M1



Place Near DRAM M2



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PEGATRON		Title : GPU_XXX	
Pegatron Corp.		Engineer: EE	
Size B	Project Name Nebula		Rev A00
Date: Wednesday, March 27, 2019		Sheet	60 of 96

www.teknisi-indonesia.com

PEGATRON		Title : GPU_XXX	
Pegatron Corp.		Engineer: EE	
Size B	Project Name Nebula		Rev A00
Date: Wednesday, March 27, 2019		Sheet	61 of 96

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PEGATRON		Title : GPU_XXX	
Pegatron Corp.		Engineer: EE	
Size B	Project Name Nebula		Rev A00
Date: Wednesday, March 27, 2019		Sheet	62 of 96

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PEGATRON

Pegatron Corp.

Title : GPU_XXX

Engineer: EE

Size B	Project Name Nebula	Rev A00
Date: Wednesday, March 27, 2019		Sheet 63 of 96

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PEGATRON		Title : GPU_XXX	
Pegatron Corp.		Engineer: EE	
Size B	Project Name Nebula		Rev A00
Date: Wednesday, March 27, 2019		Sheet 64	of 96

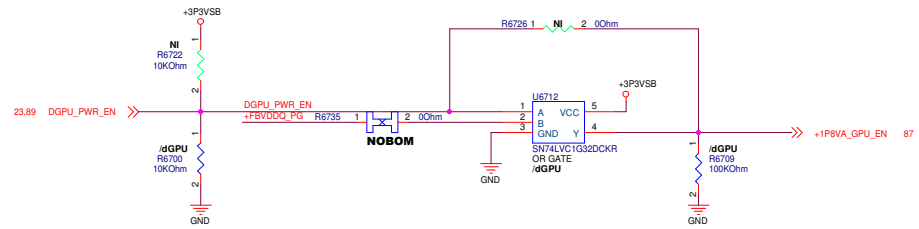
www.teknisi-indonesia.com

PEGATRON		Title : GPU_XXX	
Pegatron Corp.		Engineer: EE	
Size B	Project Name Nebula		Rev A00
Date: Wednesday, March 27, 2019		Sheet	65 of 96

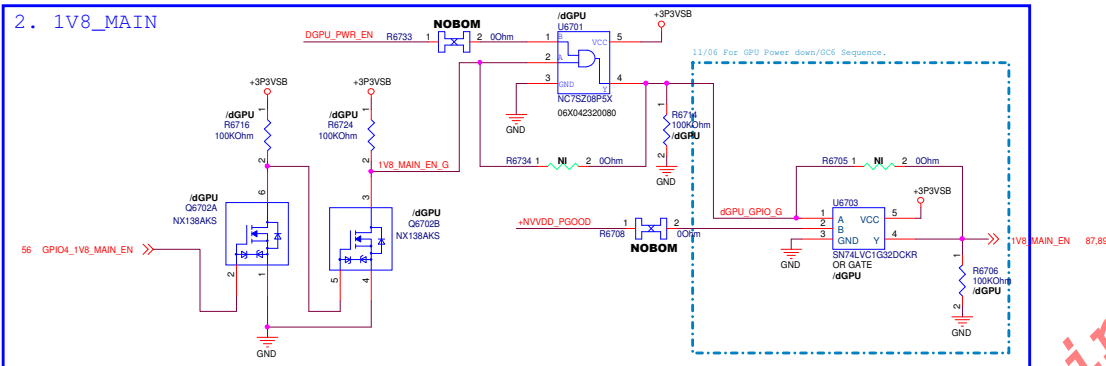
www.teknisi-indonesia.com

PEGATRON		Title : GPU_XXX	
Pegatron Corp.		Engineer: EE	
Size B	Project Name Nebula		Rev A00
Date: Wednesday, March 27, 2019		Sheet 66	of 96

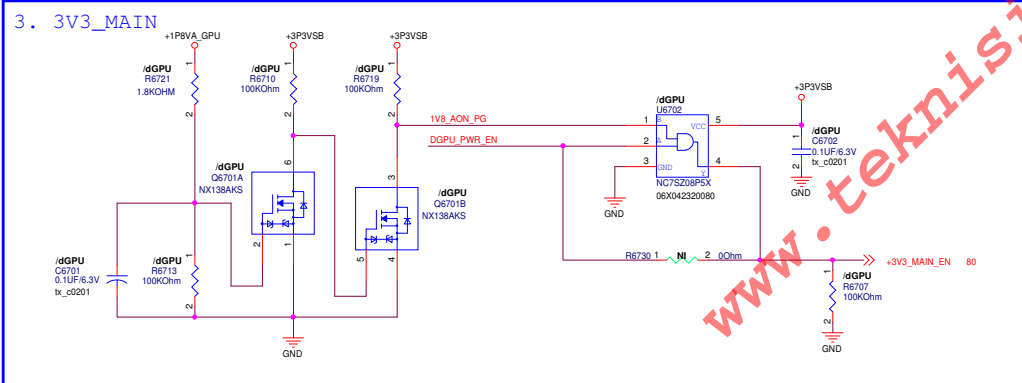
1. 1V8_AON



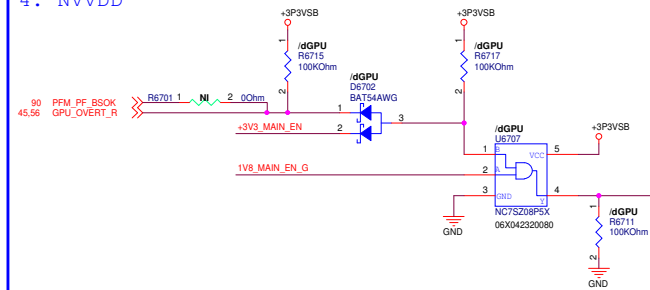
2. 1V8_MAIN



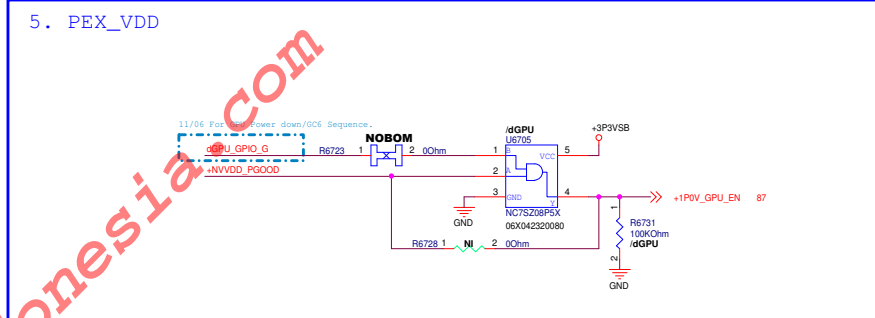
3. 3V3_MAIN



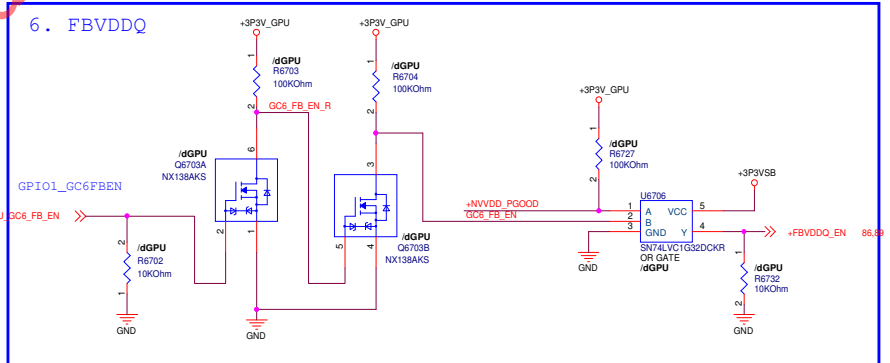
4. NVVDD



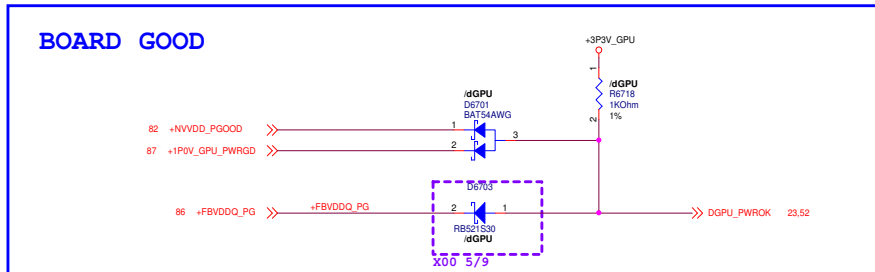
5. PEX_VDD



6. FBVDDQ

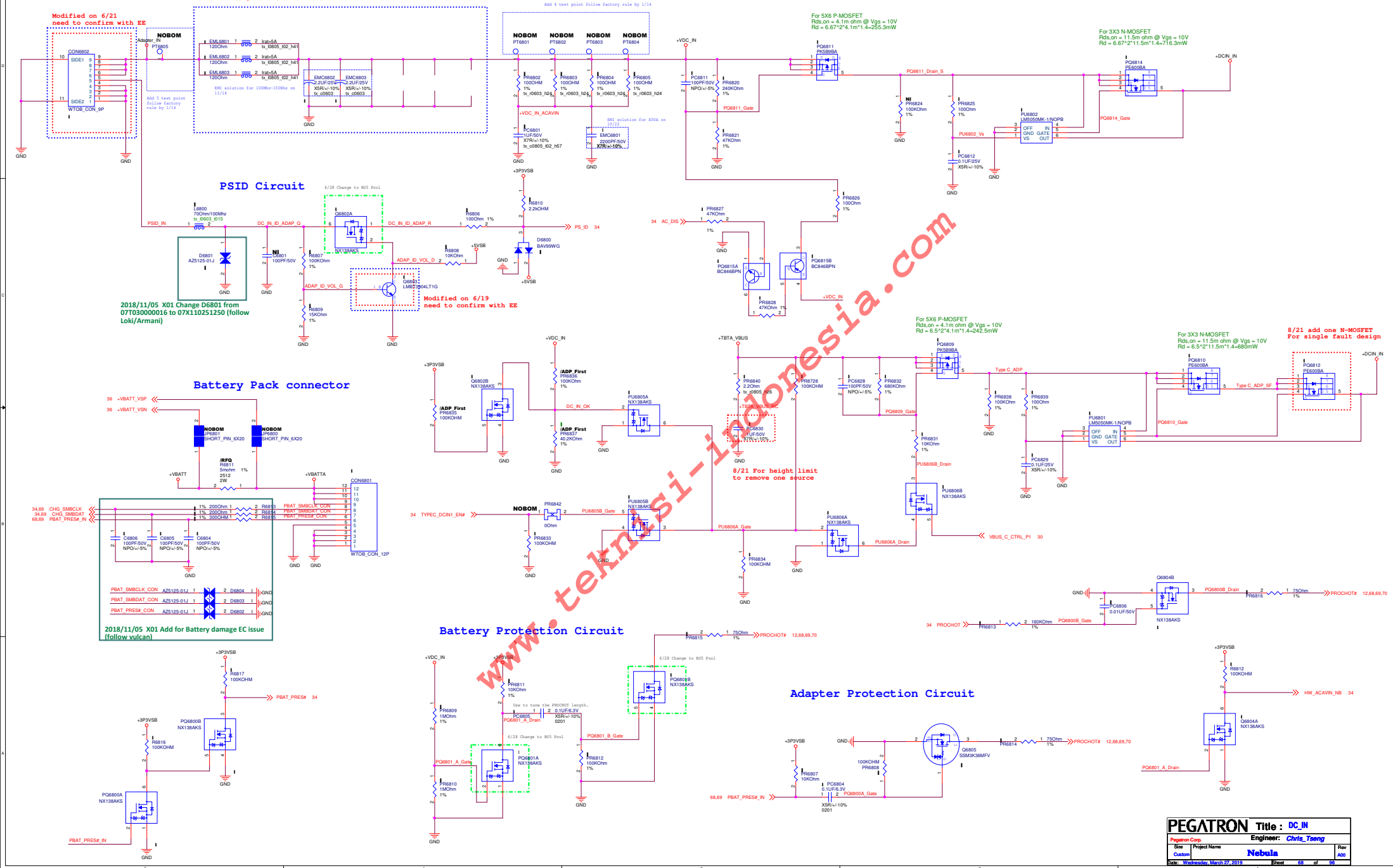


BOARD GOOD



$$N : I_{in} = 130W / 19.5V \\ = 6.667A$$

Modified on 7/12
EMI resolution
Follow Vulcan, remove all MLCC and TVS





8/9 Layout requirement
Need to add ground via beside the ground pad

Modified on 7/23
for PCB area limitation

Modified on 6/1

Modified on 7/12
EMI solution follow Vulcan
90W/9V/85%/1.5A = 7.84 pcs
=> 8 pcs

VCORE H62
I_{max}=128A
TDC=80A

VCORE H82
I_{max}=140A
TDC=86A

F_{sw} = 500kHz
I_{in} = 10.19A
Eff=84.32%
H/S=1.194*4W
L/S=1.705*4W
DC_LL: 1.8mohm

F_{sw} = 500kHz
I_{in} = 11.76A
Eff=83.43%
H/S=1.277*4W
L/S=1.887*4W
DC_LL: 1.8mohm

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : **Vcore Driver-1**

Pegatron Corp. Engineer: **Chris Tseng**

Size Project Name **Nebula** Rev A00

Date: Wednesday, March 27, 2019 Sheet 71 of 96

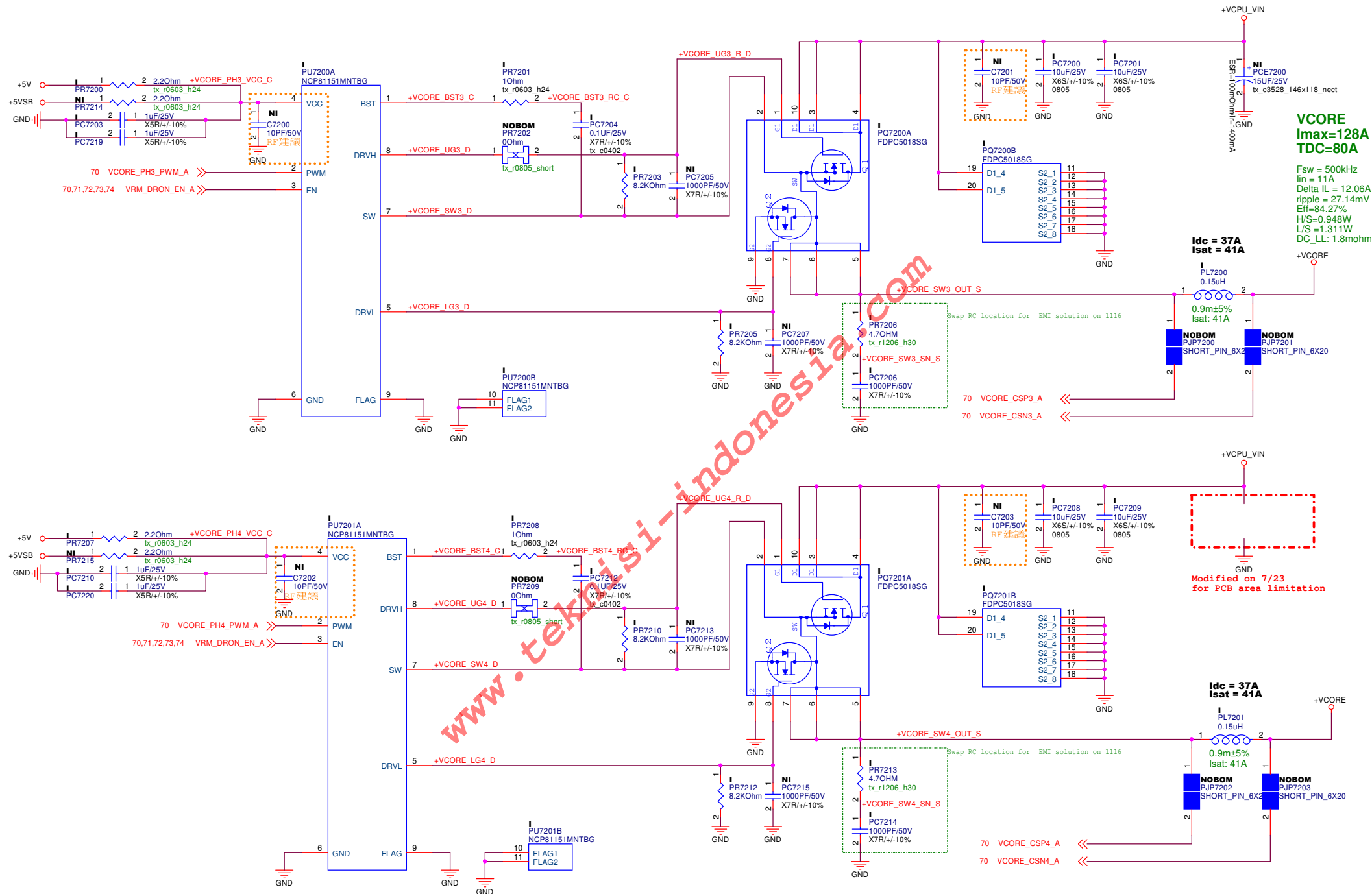
OWNER	+VCORE OC Point	Low Limit	High Limit
	167.94A -- 100% 251.91A -- 150%	78.44A	L= 0.08uH @ 80A (Per Choke)
	167.94A -- 100% 251.91A -- 150%	78.44A	L= 0.08uH @ 80A (Per Choke)

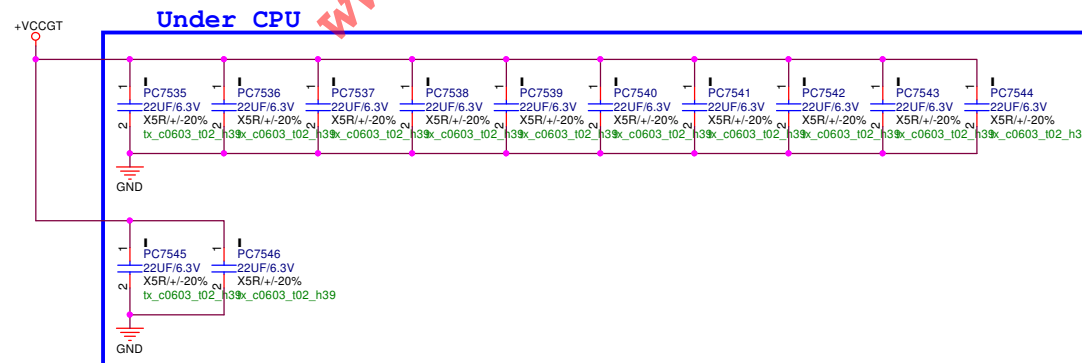
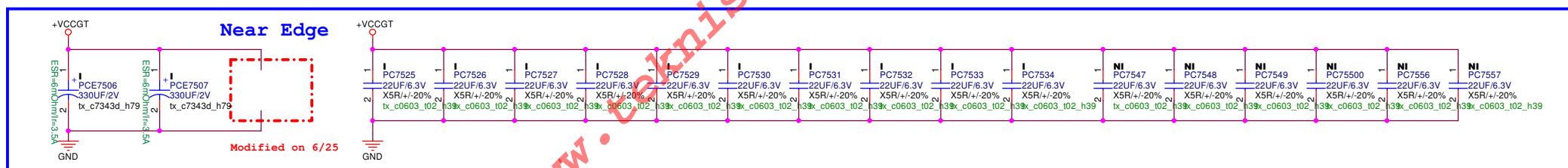
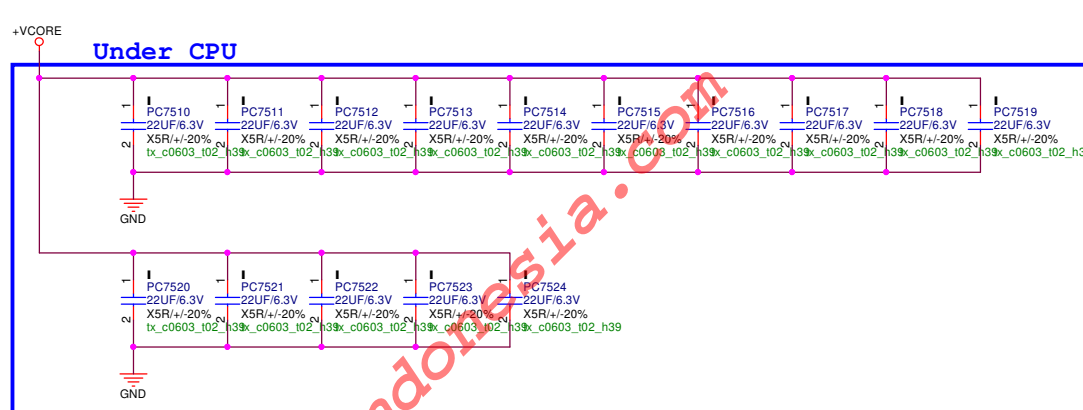
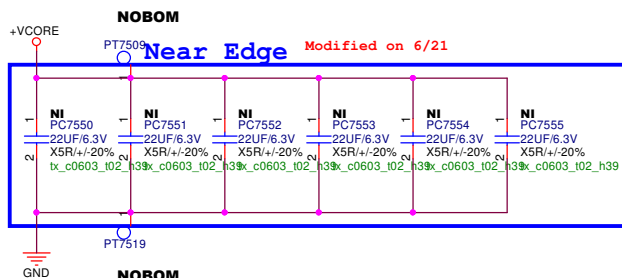
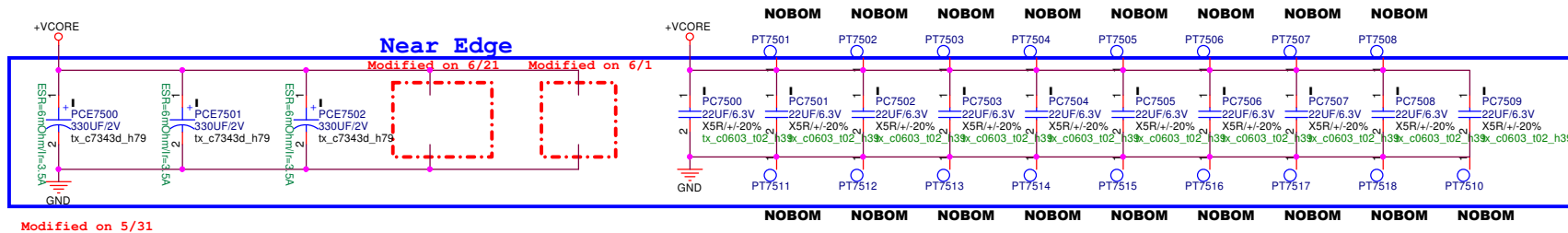
$$I_{Low Limit} = I_{DVID} + I_{o_Cout}$$

$$= 26A + (30mV/uS) * 1748uF$$

$$= 78.44A$$

※ Controller will shut down after 50uS when 184.99A ≤ I_{out} < 277.49A
Controller will shut down immediately when I_{out} trigger 277.49A





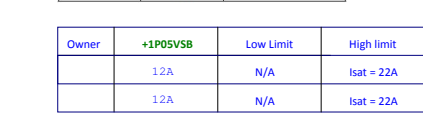
VCCGT Output CAP
 330uF/2V/H=2mm * 2 (I)
 22uF * 22 (I)
 22uF * 6 (NI)

79 +1P05VSB_+1P8VSB_EN >> **NOBOM** 1 2 00hm +1P05VSB_EN_A

GND 2 1 0.1uF/6.3V XSR +/-10% 0201

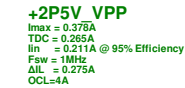
PC7602

24,45 1P05VSB_PWRGD <<

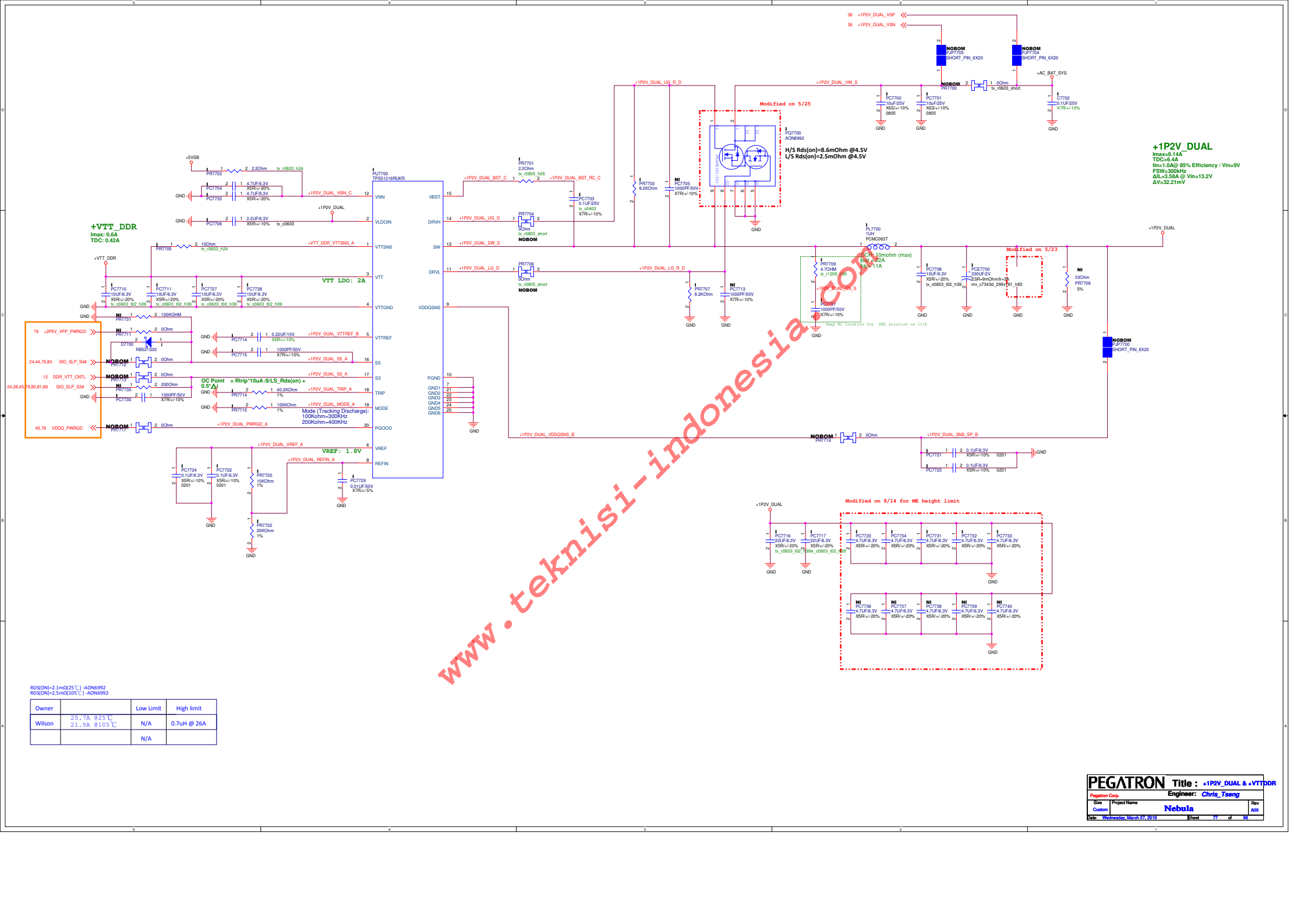




Owner	+1P05VSB	Low Limit	High limit
	12A	N/A	Isat = 22A
	12A	N/A	Isat = 22A



※ OC point is based on peak inductor current



+1P2V_DUAL
Imax=9.14A
TDC=6.4A
Ims=1.0A@85% Efficiency / Vims9V
FSW=300kHz
dIL=3.58A @ Vins=13.2V
AV=32.21mV

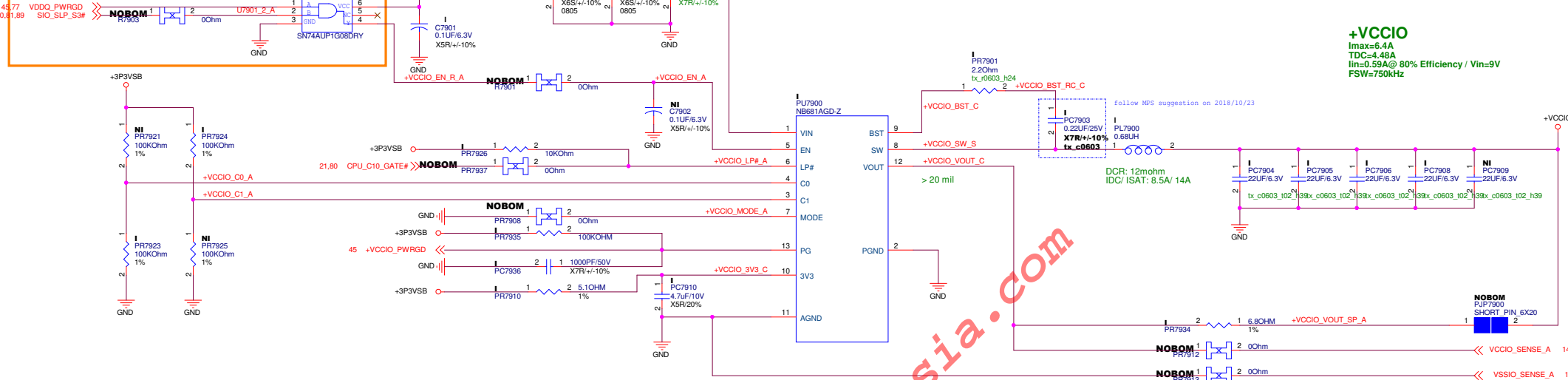
+VTT_DDR
Imax=0.6A
TDC=0.42A

76 +2PSV_VPP_PWRGD
24.44,76,80 SIO_SLP_S44
12 DOR_VTT_CNTL
24.28,45,79,80,81,89 SIO_SLP_S34
45.79 VDDQ_PWRGD

OC Point = $R_{trip} \cdot I_{0uA} / (LS \cdot R_{ds(on)} + 0.5A)$
Mode (Tracking Discharge):
100Kohm=300KHz
200Kohm=400KHz

RDS(ON)=2.1mQ(25°C) -ADN6992 RDS(ON)=2.5mQ(105°C) -ADN6992			
Owner		Low Limit	High limit
Wilson	25.7A @25°C 21.9A @105°C	N/A	0.7uH @ 26A
		N/A	

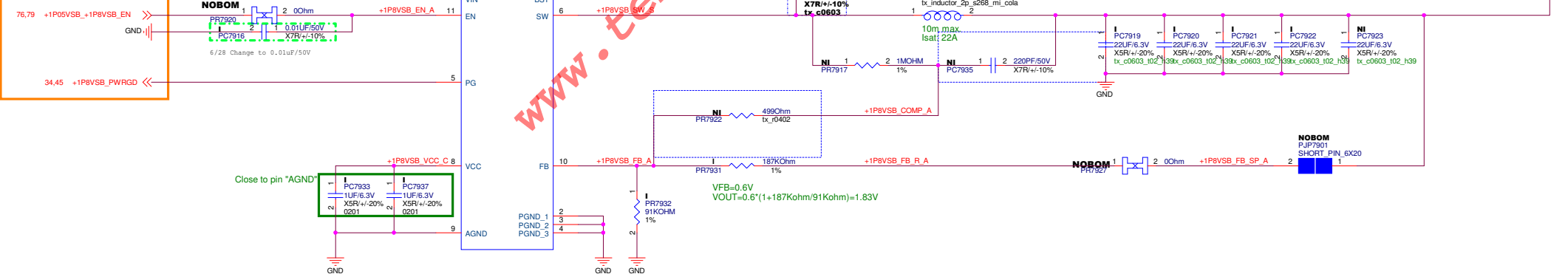
EE need to check sequence



+VCCIO
 Imax=6.4A
 TDC=4.48A
 Iin=0.59A@ 80% Efficiency / Vin=9V
 FSW=750kHz

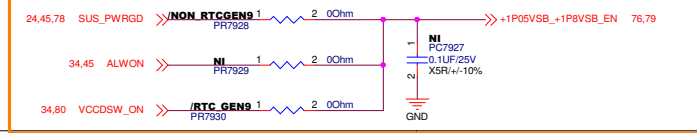
Owner	+VCCIO OC point (Valley point)	Low Limit	High limit
	7.5A	N/A	L_Isat = 14A

EE need to check sequence



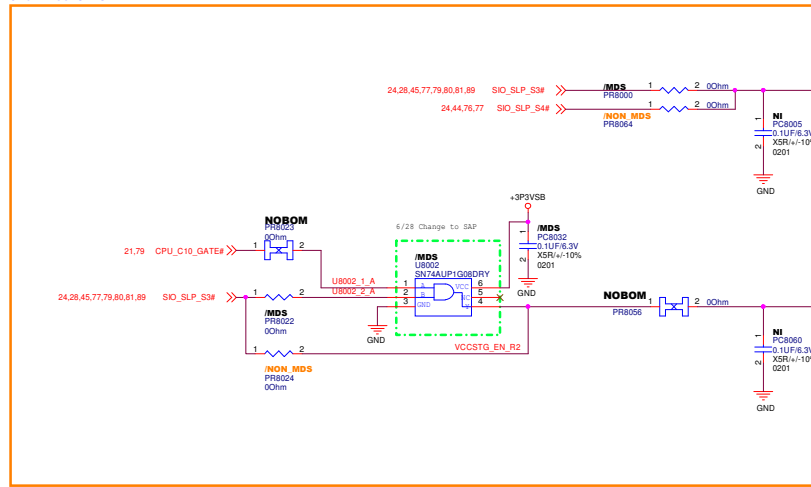
+1P8VSB
 Imax=1.97A
 TDC=1.38A
 Iin=0.32A@ 86% Efficiency / Vin=9V
 FSW=750kHz

EE need to check sequence



Owner	+VCCIO OC point (Valley point)	Low Limit	High limit
	7.5A	N/A	L_Isat = 22A

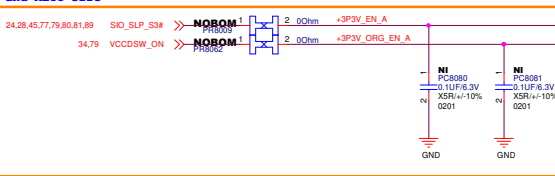
EE need to check sequence and MLCC size



+VCCST
 $I_{max} = 0.21A$
 $TDC = 0.147A$
 $RDS(ON) = 9.5m\ ohm$
 $Pd = 0.287mW$
 $Vdrop = 2.8mV$

+VCCSTG
 $I_{max} = 0.02A$
 $TDC = 0.014A$
 $RDS(ON) = 9.5m\ ohm$
 $Pd = 0.002mW$
 $Vdrop = 0.266mV$

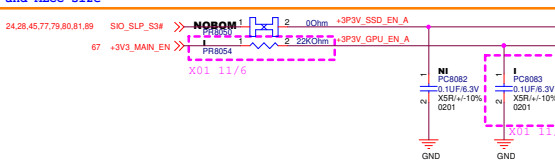
EE need to check sequence and MLCC size



+3P3V
 $I_{max} = 1.6A$
 $TDC = 1.12A$
 $RDS(ON) = 24m\ ohm$
 $Pd = 42mW$
 $Vdrop = 53.76mV$

+3P3V_ORG
 $I_{max} = 0.24A$
 $TDC = 0.168A$
 $RDS(ON) = 24m\ ohm$
 $Pd = 1.94mW$
 $Vdrop = 8mV$

EE need to check sequence and MLCC size



+3P3V_SSD
 $I_{max} = 4A$
 $TDC = 2.6A$
 $RDS(ON) = 24m\ ohm$
 $Pd = 263.4mW$
 $Vdrop = 134.4mV$

+3P3V_GPU
 $I_{max} = 0.07A$
 $TDC = 0.049A$
 $RDS(ON) = 24m\ ohm$
 $Pd = 0.06mW$
 $Vdrop = 2.35mV$

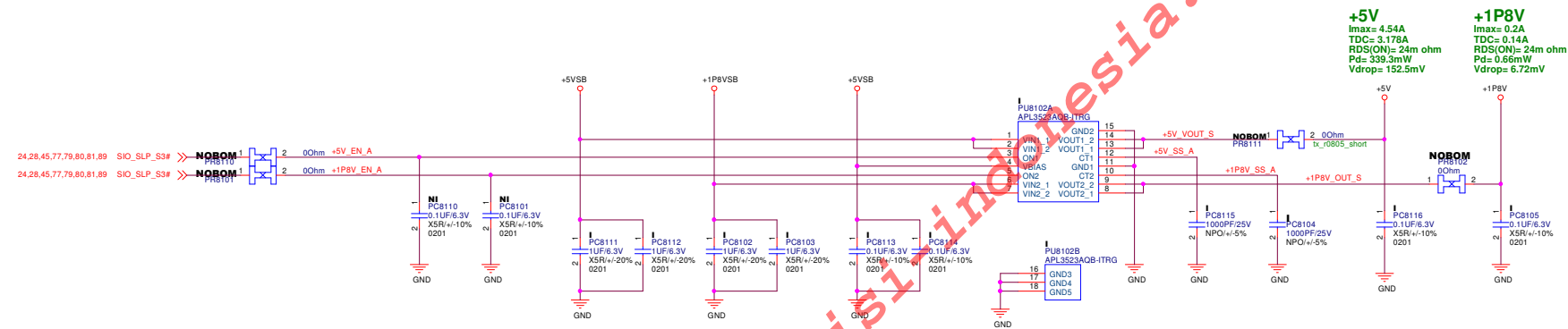
PEGATRON Title : Load switch1

Engineer : Chris Tseng

Size : Project Name : Nebula

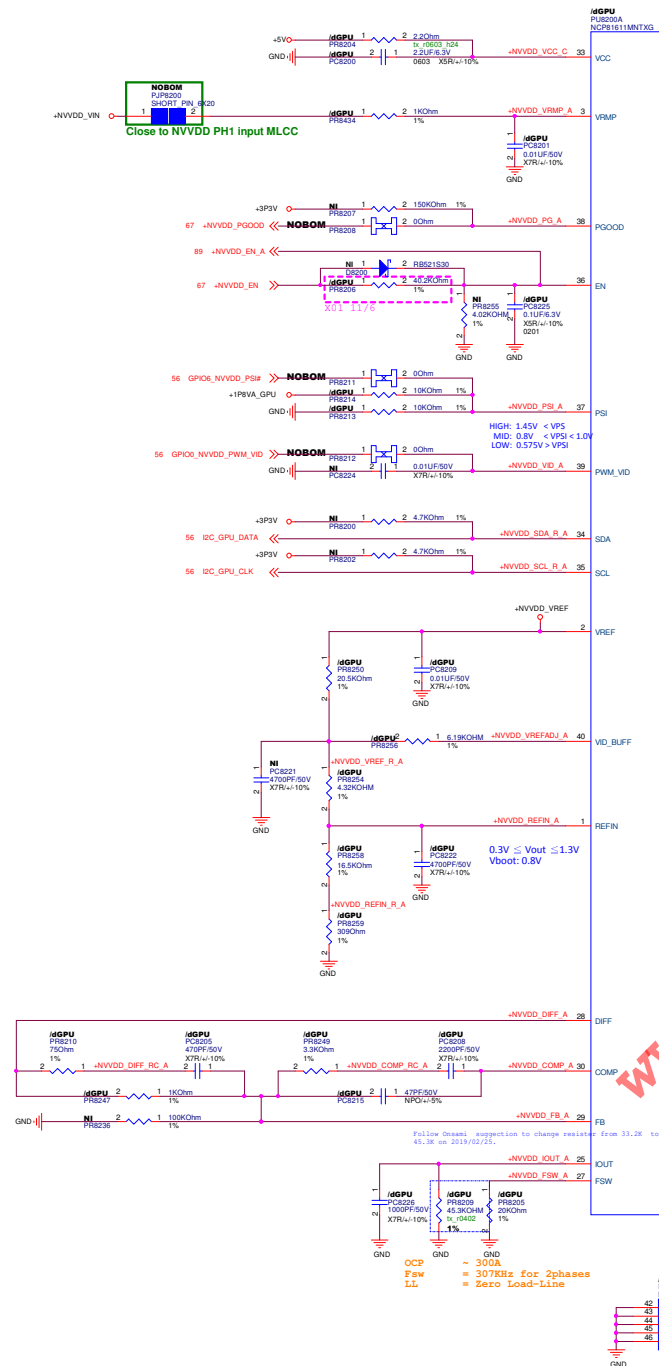
Customer : Rev : A00

Date : Wednesday, March 27, 2019 Sheet : 30 of 30



+5V
 $I_{max} = 4.54A$
 $TDC = 3.178A$
 $RDS(ON) = 24m\ ohm$
 $Pd = 339.3mW$
 $Vdrop = 152.5mV$

+1P8V
 $I_{max} = 0.2A$
 $TDC = 0.14A$
 $RDS(ON) = 24m\ ohm$
 $Pd = 0.66mW$
 $Vdrop = 6.72mV$



PEGATRON DT-MB RESTRICTED SECRET

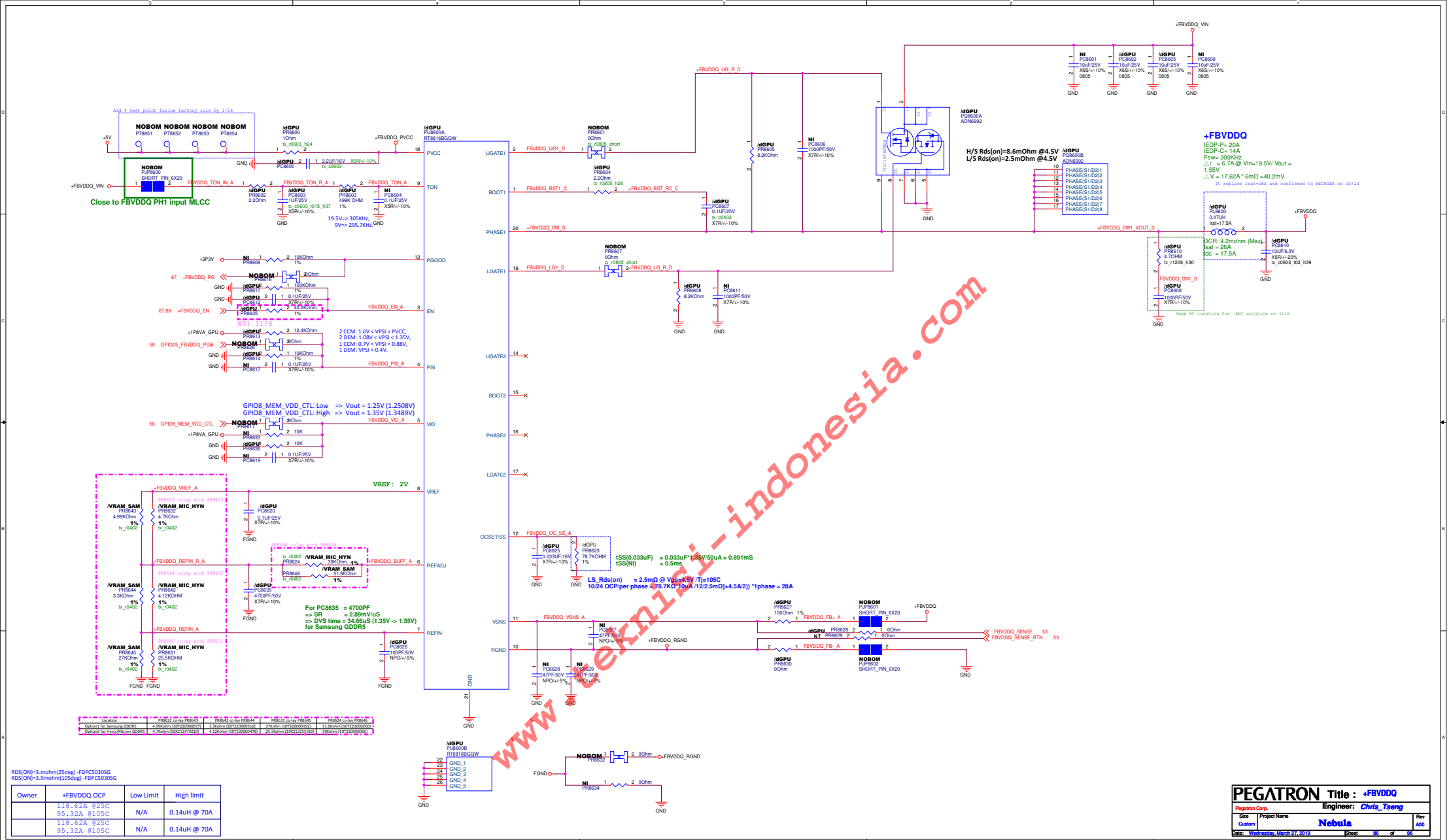
PEGATRON Title : NVVDD Controller			
Project Name		Engineer: Chris Tseng	
Size	Custom	Netbul	Rev A00
Date: Wednesday, March 27, 2019 Sheet 82 of 86			

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PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title : +NVVD Driver-3	
Pegatron Corp.		Engineer: Chris Tseng	
Size C	Project Name Nebula	Rev A00	
Date: Wednesday, March 27, 2019		Sheet 85 of 96	



330uF/2V/H=2mm * 4 (I)
330uF/2V/H=2mm * 1 (NI)

330uF/2V/H=2mmH (NI)

Modified on 2019/6/1

+NVVDD

ESR=6mOhm/I=3.5A

1

2

GND

+dGPU
PCE8802
330UF/2V
tx_c7343d_h79

ESR=6mOhm/I=3.5A

1

2

GND

+dGPU
PCE8806
330UF/2V
tx_c7343d_h79

ESR=6mOhm/I=3.5A

1

2

GND

+dGPU
PCE8807
330UF/2V
tx_c7343d_h79

ESR=6mOhm/I=3.5A

1

2

GND

+dGPU
PCE8817
330UF/2V
tx_c7343d_h79

NI
PCE8818
220UF/2V
tx_c7343_295x177_h39

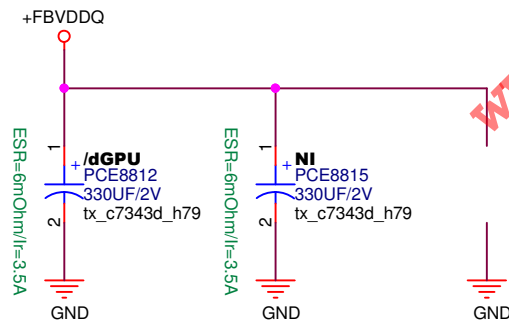
GND

Modified on 6/1

GND

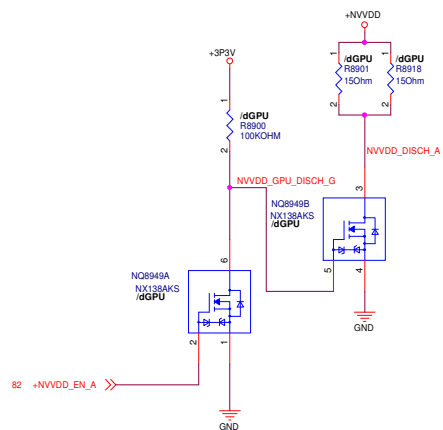
GND

330uF/2V/H=2mm * 1 (I)
330uF/2V/H=2mm * 1 (NI)

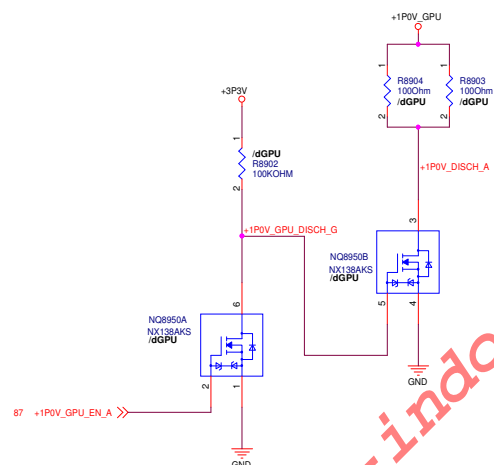


GPU POWER DISCHARGE

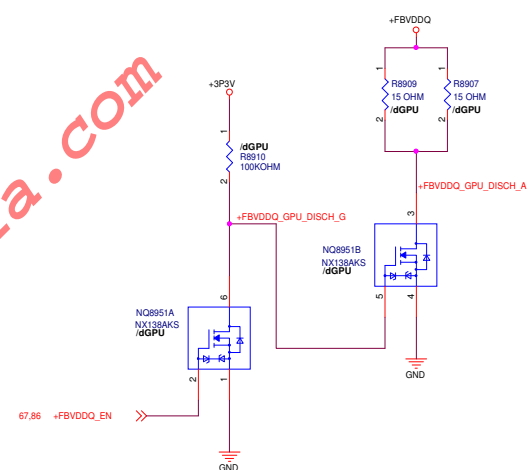
NVVDD DISCHARGE



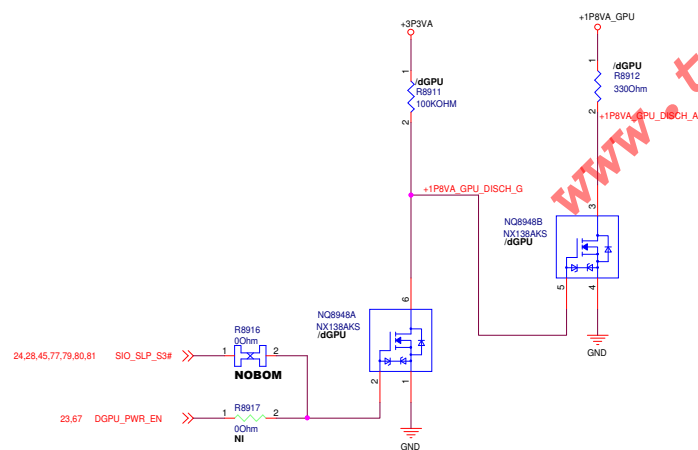
1P0V DISCHARGE



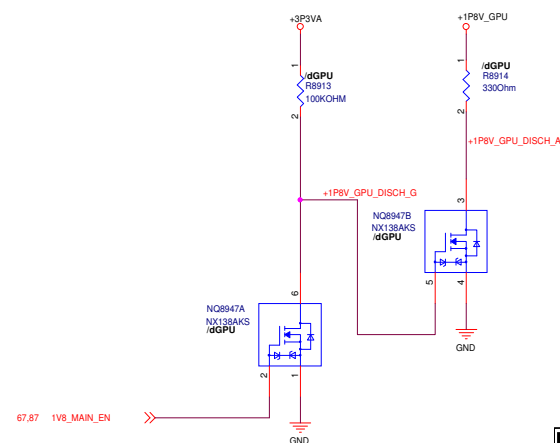
FBVDDQ DISCHARGE

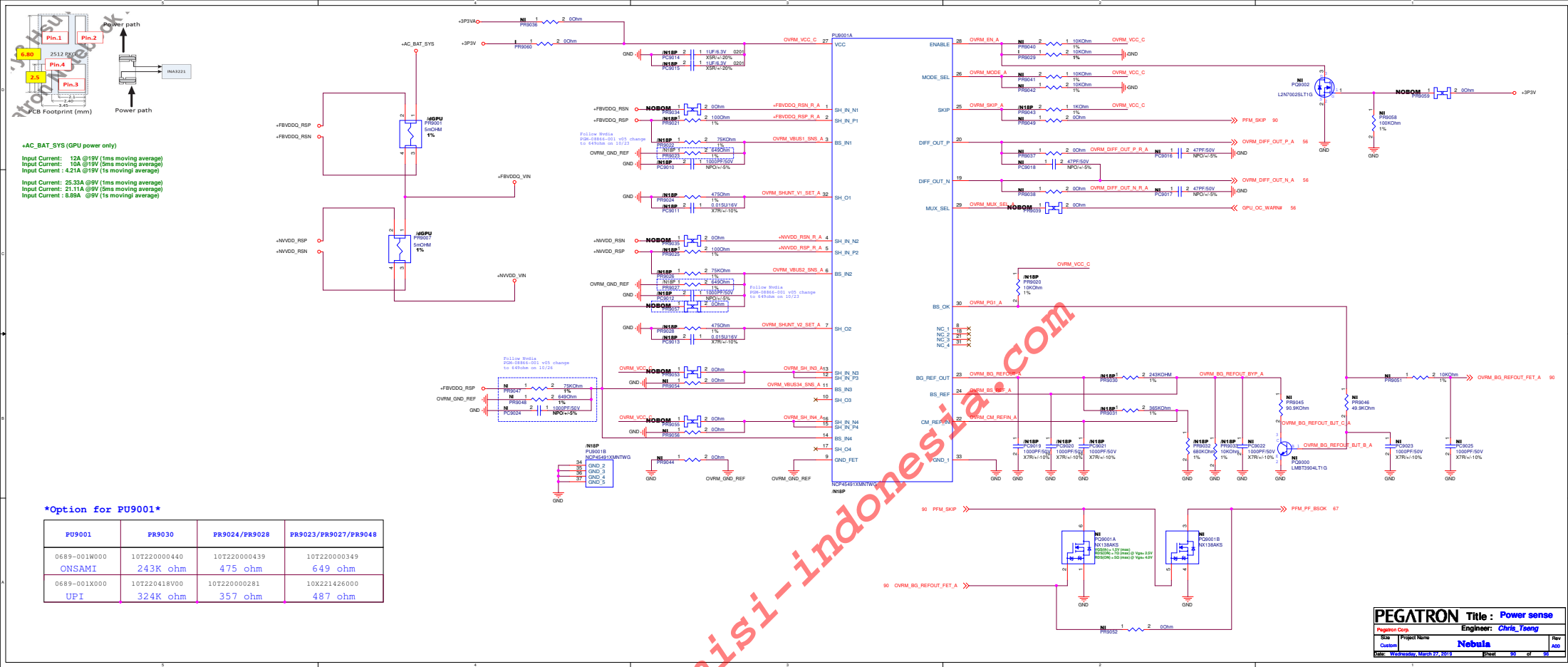


1P8VA_GPU DISCHARGE



1P8V_GPU DISCHARGE





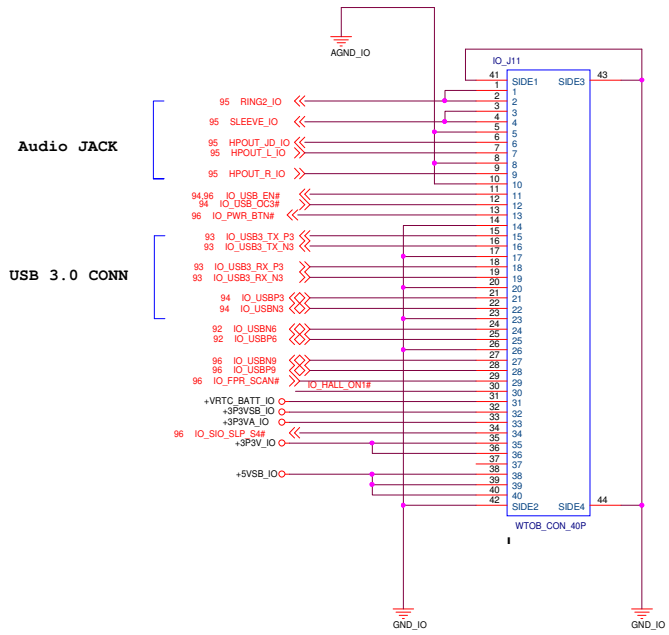
+AC_BAT_SYS (GPU power only)
Input Current: 12A @19V (1ms moving average)
Input Current: 10A @19V (5ms moving average)
Input Current: 4.21A @19V (1s moving average)
Input Current: 25.33A @9V (1ms moving average)
Input Current: 21.11A @9V (5ms moving average)
Input Current: 8.89A @9V (1s moving average)

Option for PU9001

PU9001	PR9030	PR9024/PR9028	PR9023/PR9027/PR9048
0689-001W000	10T220000440	10T220000439	10T220000349
ONSAMI	243K ohm	475 ohm	649 ohm
0689-001X000	10T220418V00	10T220000281	10X221426000
UPI	324K ohm	357 ohm	487 ohm

A01 IO CONN & Hall Sensor

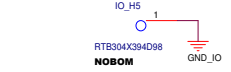
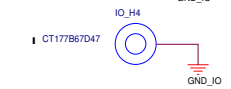
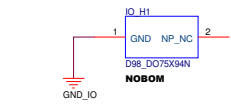
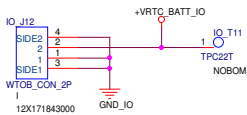
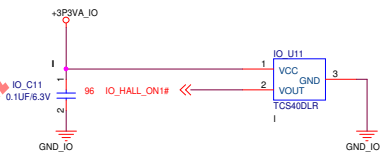
IO Connector



IO Connector Pin Define

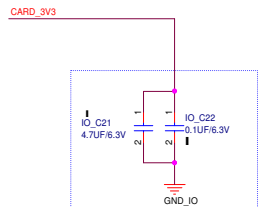
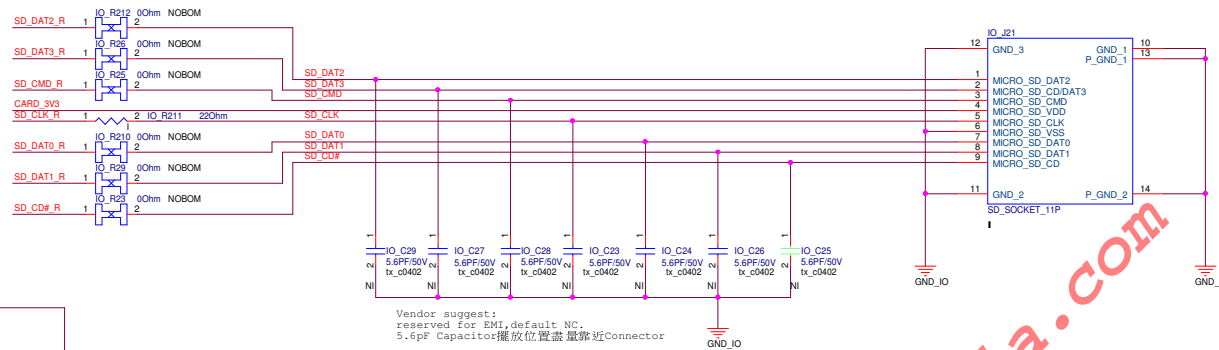
1	RING2_IO	21	IO_USBP3
2	RING2_IO	22	IO_USBN3
3	SLEEVE_IO	23	GND_IO
4	SLEEVE_IO	24	IO_USBN6
5	AGND_IO	25	IO_USBP6
6	HPOUT_JD_IO	26	GND_IO
7	HPOUT_L_IO	27	IO_USBN9
8	AGND_IO	28	IO_USBP9
9	HPOUT_R_IO	29	IO_FPR_SCAN#
10	AGND_IO	30	IO_HALL_ON1#
11	IO_USB_EN#	31	+VRTC_BATT_IO
12	IO_USB_OC3#	32	+3P3VSB_IO
13	IO_PWR_BTN#	33	+3P3VA_IO
14	GND_IO	34	NC
15	IO_USB3_TX_P3	35	+3P3V_IO
16	IO_USB3_TX_N3	36	+3P3V_IO
17	GND_IO	37	NC
18	IO_USB3_RX_P3	38	+5VSB_IO
19	IO_USB3_RX_N3	39	+5VSB_IO
20	GND_IO	40	+5VSB_IO

Hall Sensor

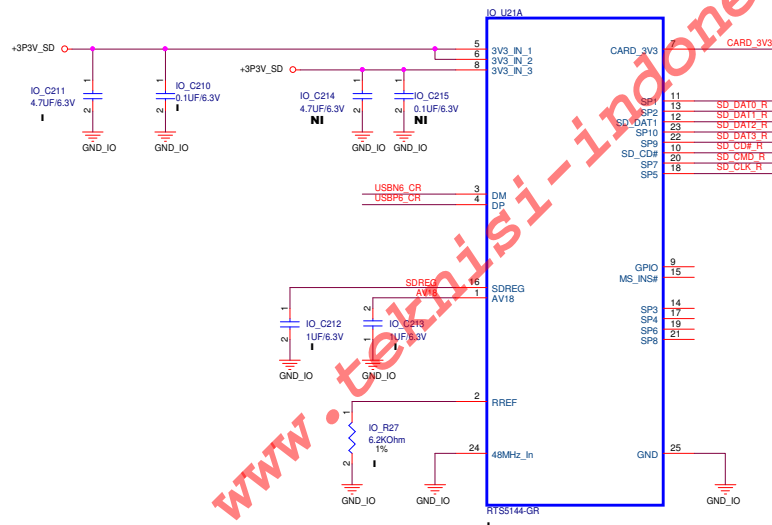
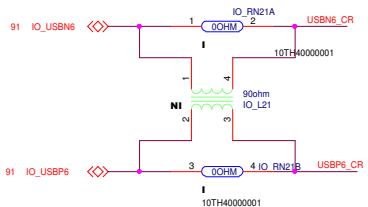
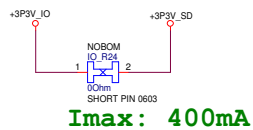


For Power button standoff
11/09 Change to 1308-00W8000

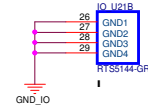
A02 Card_reader_RTS5144-GR



POWER

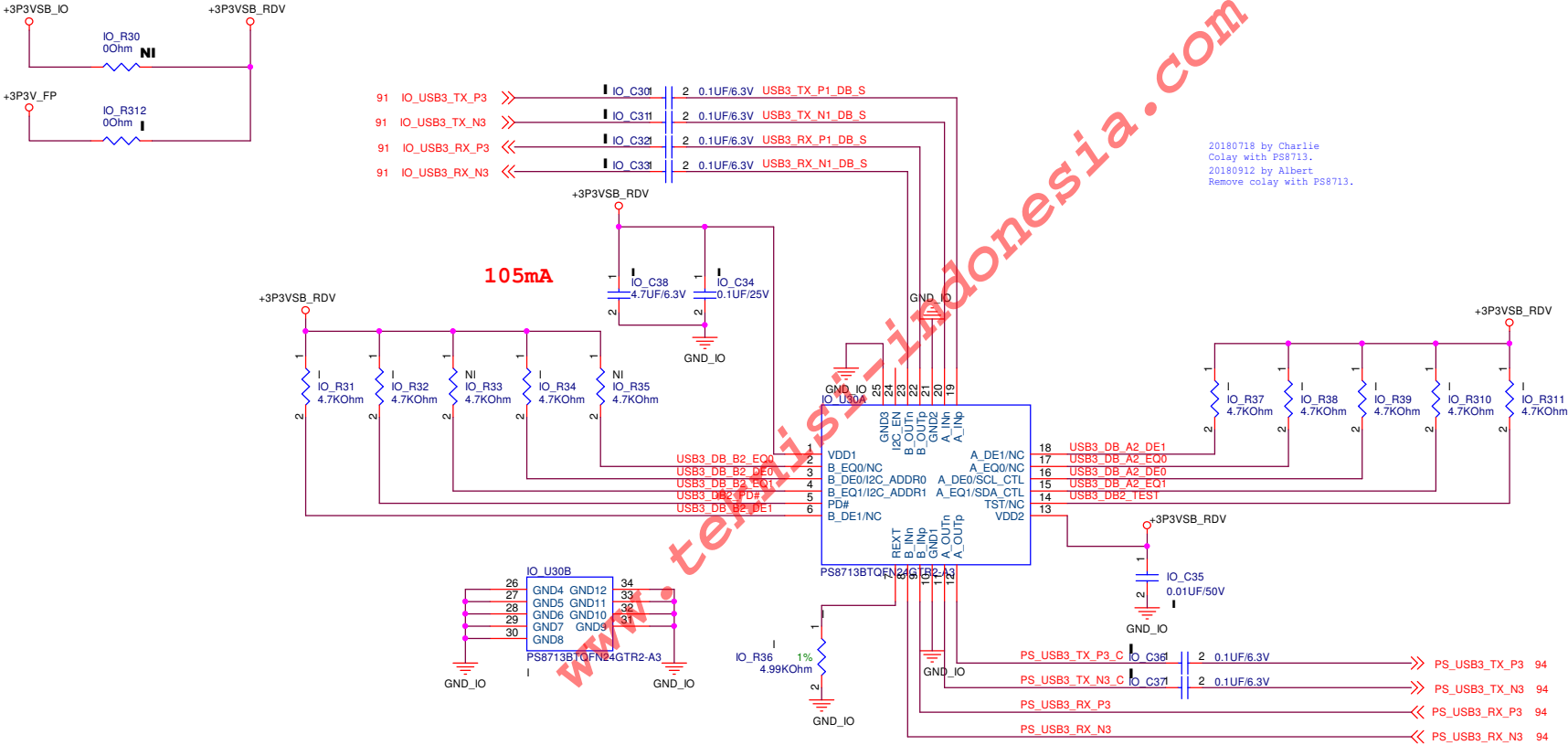


card lock	SD_WP pin high
card unlock	SD_WP pin low

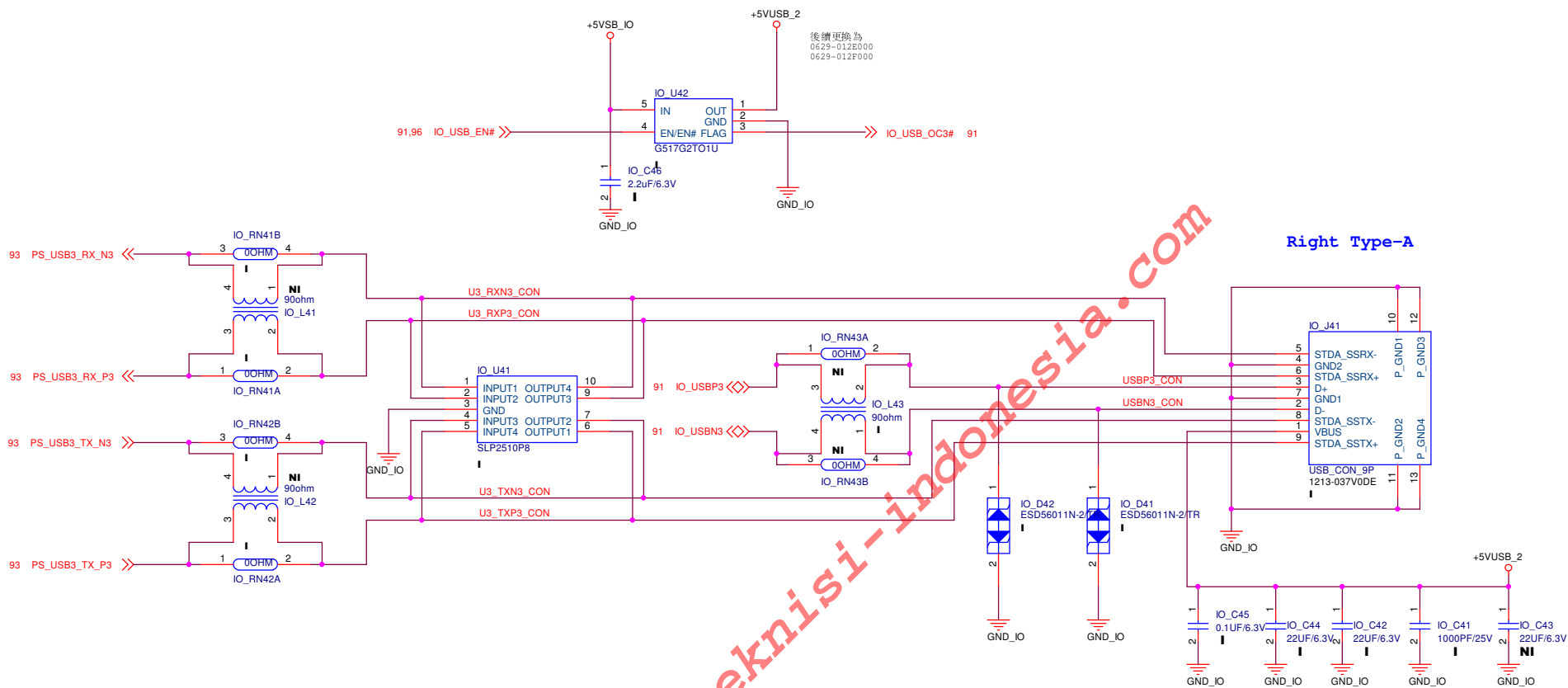


A03 USB3.1 TypeA Port1 & Repeater (IO Board)

I_{max}: 105mA



A04 USB3.1 TypeA Port1 & Repeater (IO Board)

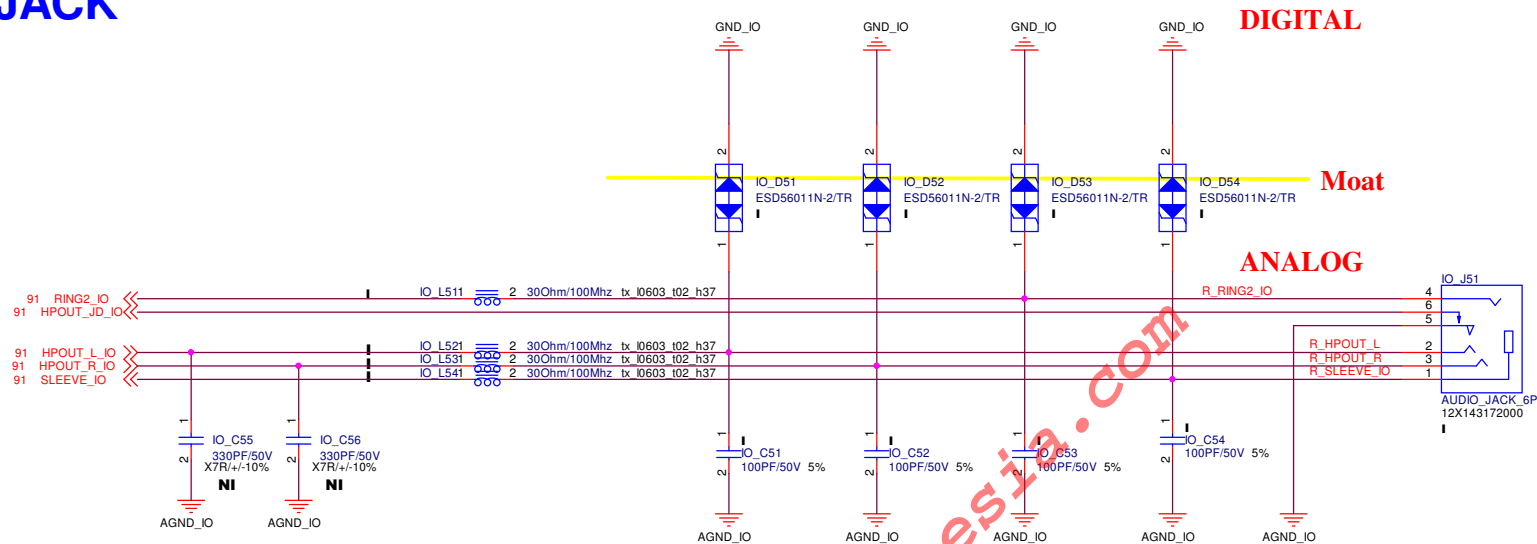


<Core Design>

PEGATRON Title : USB CONN & POWER
Pegatron Corp. Engineer: Albert2_Liu

Size	Project Name	Rev
A3	Nebula	A00
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A05 AUDIO JACK



GLOBAL HEADSET CONNECTOR

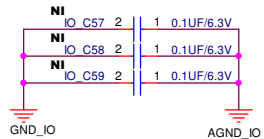
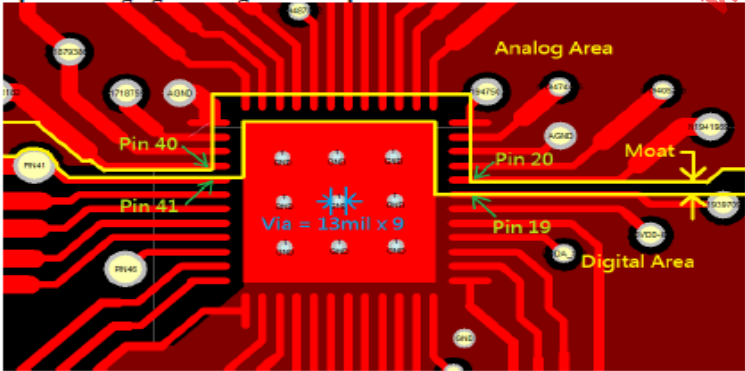
OMTP/CTIA headset, Headphone, Line-Out, Microphone input, Line input.

Below figures are 4-pole jack plugged to the combo phone jack, we could see that right figure's HP-JD pins(#5/#6) attached to HP-L(#1), that imply headset jack has to be fully plugged to make HP JD trigger. This kind of connector will significantly decrease the chance of wrong judgment. Below left figure is not the recommended phone-jack, because its HP-JD(#3/#4) attached to HP right channel.

PCB trace width of Mic1-R/Mic1-L(SLEEVE/RING2) are required at least 40 mil for HP crosstalk consideration, and its length should be as short as possible.

FB1/FB2 should choose DC resistance (Rdc) < 30mOhm to get the best audio performance for HP crosstalk.

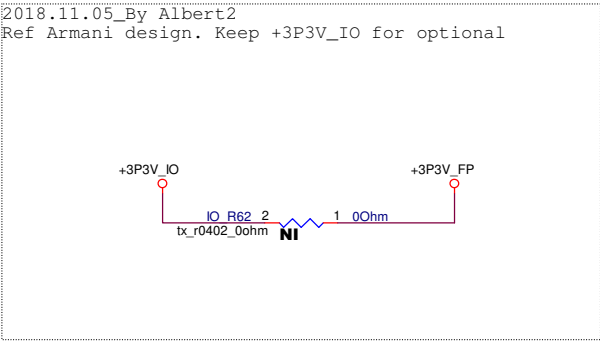
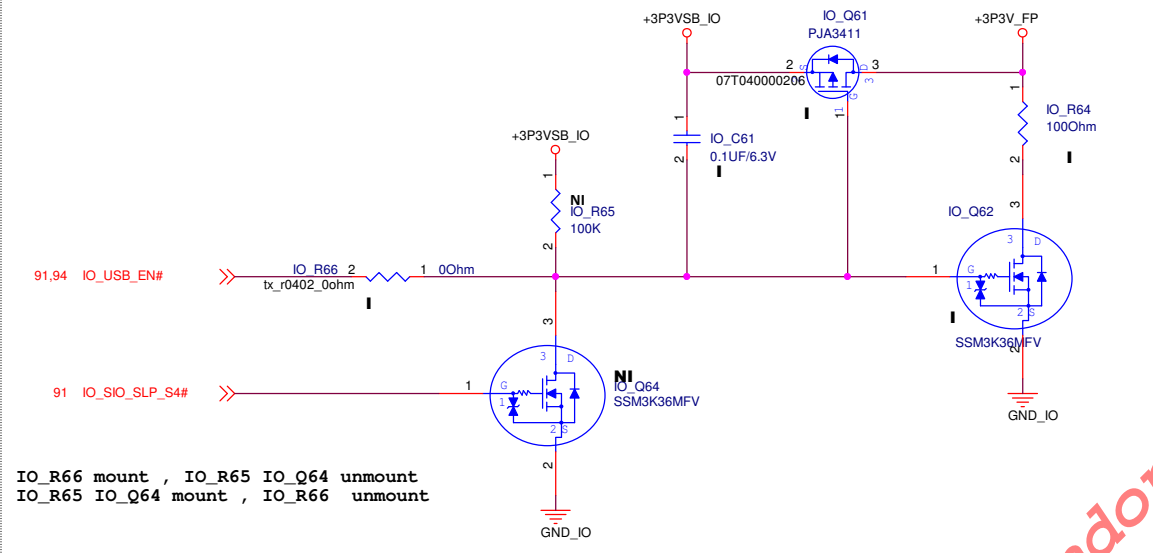
Separate Analog and Digital GND plane



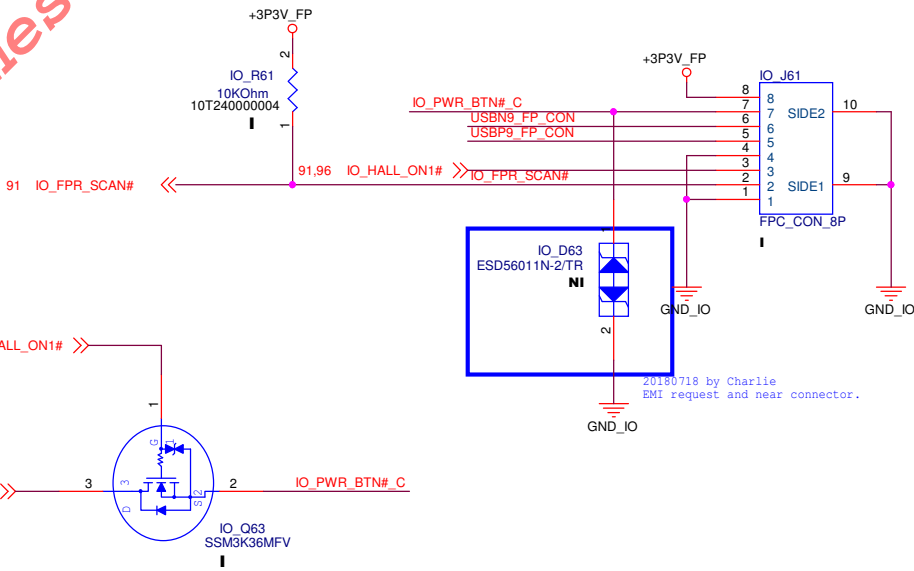
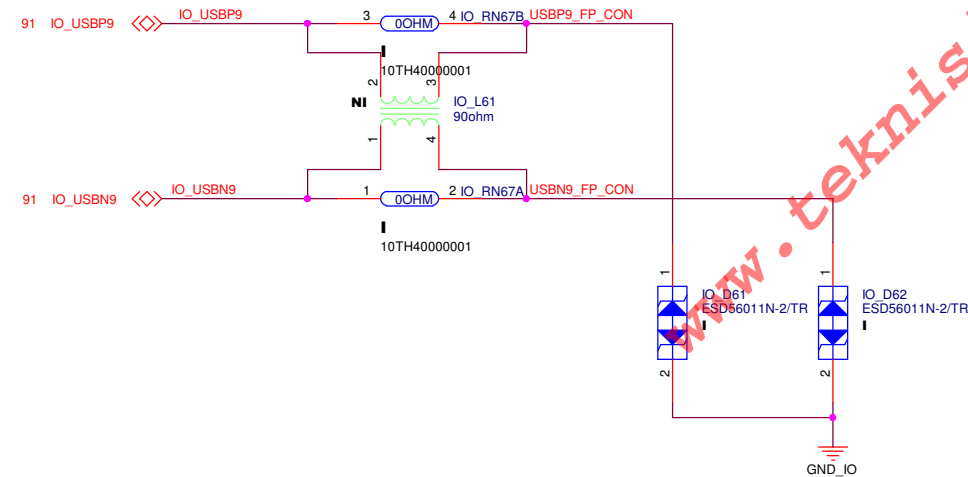
<Core Design>			
PEGATRON		Title : AUDIO JACK	
Pegatron Corp.		Engineer: Steven_Diau	
Size	Project Name	Rev	
A3	Nebula	A00	
Date: Wednesday, March 27, 2019		Sheet	95 of 96

A06 Finger Print

2018.11.13_By Albert2
Customer demand
-> FP S3 state keep power on (S4 no power)



FPR CONNECTOR



<Core Design>		Title : IO Conn	
PEGATRON		Engineer: Albert2_Liu	
Pegatron Corp.		Project Name	
Size		Rev	
B		A00	
Date: Wednesday, March 27, 2019		Sheet 96 of 96	